Code No: X0524/R07 **Set No. 1**

II B.Tech I Semester Supplementary Examinations, November 2012
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Convert the following to Decimal and then to Octal.
   (a) 1234_{16}
   (b) $12EF_{16}$
   (c) 10110011_2
   (d) 10001111_2
   (e) 352_{10}
   (f) 999_{10} [3+3+3+3+2+2]

2. (a) Write short notes about the various digital logic families.
   (b) Obtain the complement of the following Boolean expressions.
      i. AB + A(B + C) + B'(B + D)
      ii. A + B + A'B'C.
   (c) Obtain the dual of the following Boolean expressions.
      i. A'B + A'BC' + A'BCD + A'BC'D'E
      ii. ABEF + ABE'F' + A'B'EF. [8+4+4]

3. (a) Draw the multiple level NOR circuit for the following expression: $A(B + C + D) + BCD$
   (b) Simplify the following functions and implement two level NOR gates: [8+8]
      i. $f(A, B, C, D) = \Sigma 0, 2, 4, 6, 8, 9, 10, 11, 12$
      ii. $F(w, x, y, z) = \Sigma 5, 6, 9, 11$

4. (a) If $F_1(A, B, C, D) = \Sigma(1, 3, 4, 5, 9, 10, 11) + d(6, 8)$ and $F_2(A, B, C, D) = \Pi(1, 3, 5, 6, 10, 11, 13, 14) + d(9, 12)$
   Design a minimal SOP logical circuit for $F_3(A, B, C, D) = F_1 \oplus F_2$
   Draw the circuit using NOR- gates.
   (b) Design a Code converter circuit to convert 9's complement code to BCD code using Full-adders and additional gates. (Use block diagram of Full adders). [8+8]

5. A sequential circuit with 3 D-flip-flops A, B and C has only one input 'X' and one output 'X' with following relationship
   $D_A = B \oplus C \oplus X, \quad D_B = A, \quad D_C = B$

(a) Draw the logic diagram of the circuit.

(b) Obtain logic diagram, state table and state diagram. [16]

6. (a) What is the maximum frequency required for a 10-bit ripple counter and synchronous counter, if the propagation delay of the flip flop is 10ns.

(b) Design a clocked sequential circuit to detect 1111 or 0000. Overlapping is allowed. Draw the circuit using flip flops. [6+10]

7. (a) Give the HDL code for a memory read , write operations if the memory size is 64 words of 4 bits each. Also explain the code

(b) Obtain the 15-bit Hamming code for the 11-bit data word 11001001010. [8+8]

8. (a) Explain critical and non critical races with the help of examples.

(b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are: [6+10]

$$Y1 = x_1x_2 + x_1y_2' + x_2'y_1$$
$$Y2 = x_2 + x_1y_1'y_2 + x_1'y_1$$
$$Z = x_2 + y_1$$

i. Draw the logic diagram of the circuit.

ii. Derive the transition table and output map.

iii. Obtain a flow table for the circuit.

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Code No: X0524/R07 **Set No. 2**

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1. (a) Explain different methods used to represent negative numbers in binary system. [6]
   (b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. [5×2]
      i. 11010 - 10010
      ii. 11011-1101
      iii. 100-110000
      iv. 1010100-1010100
      v. 11-1011.

2. (a) Reduce the following Boolean Expressions.
      i. AB + A(B + C) + B'(B + D)
      ii. A +B + A'B'C
      iii. A'B + A'BC' + A'BCD + A'BC'D'E
      iv. ABEF + AB(EF)' + (AB)'EF.
   (b) Obtain the Dual of the following Boolean expressions.
      i. x'yz'+ x'yz' + xy'z' + xy'z
      ii. x'yz + xy'z' + xyz + xyz'
      iii. x'z + x'y + xy'z + yz
      iv. x'y'z' + x'yz' + xy'z' + xy'z + xyz'. [8+8]

3. (a) Construct K-map for the following expression and obtain minimal SOP expression. Implement the function with 2-level NAND -NAND form.
   $f(A,B,C,D) = (A+C+D)\left(A+B+\overline{D}\right)\left(A+B+\overline{C}\right)\left(\overline{A}+B+\overline{D}\right)\left(\overline{A}+B+\overline{D}\right)$
   (b) Implement the following Boolean function F using the two - level form:
      i. NAND-AND
      ii. AND-NOR $F(A,B,C,D) = \Sigma 0,1,2,3,4,8,9,12$ [8+8]

4. (a) Using five lower - order demultiplexer, construct 6 to 64 line demultiplexer circuit. Use only block diagrams.
   (b) Design a Combinational logic circuit with three inputs A, B, C and three outputs x, y, z. If the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input. Draw the circuit using three-2 input AND gates, one 3 input OR gate, one 3 input X - OR gate and one inverter. [4+12]

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5. (a) Draw the circuit diagram of clocked D- flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram.
   (b) Explain the procedure for the design of sequential circuits with example. [8+8]

6. A counter is to be designed to count either in 5421 code or 8421 code based on a control signal input. Draw the state diagram for such a counter and synthesize it using T flip flops. Assume that the control signal cannot change in the middle of a counting sequence. [16]

7. (a) What is parity checking? Explain its necessity and how is it implemented?
   (b) If the Hamming code sequence 1100110 is transmitted & due to error in one position, is received as 1110110, locate the position of the error bit using parity checks and give the method for obtaining the correct sequence. [8+8]

8. (a) Describe the operation of the SR Latch using NAND gate with the help of truth table, transition table and the circuit.
   (b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are:
   Y1 = $x_1x_2 + x_1y_2' + x_2'y_1$
   Y2 = $x_2 + x_1y_1'y_2 + x_1'y_1$
   z= $x_2 + y_1$ Implement the circuit defined above with NAND SR latches. [8+8]

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Code No: X0524/R07 **Set No. 3**

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1. (a) Explain, How error occurred in a data transmission can be detected using parity bit. [6]
   (b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. [5×2]
      i. 111011 - 111000
      ii. 1110-110110
      iii. 10010-1101
      iv. 110-10100
      v. 11011-10000.

2. (a) Explain in detail, the various levels of integration in ICs.
   (b) Obtain the Dual of the following Boolean expressions.
      i. AB + A(B + C) + B'(B + D)
      ii. A + B + A'B'C.
   (c) Obtain the complement of the following Boolean expressions. [8+4+4]
      i. A'B + A'BC' + A'BCD + A'BC'D'E
      ii. ABEF + ABE'F' + A'B'EF.

3. (a) Implement the following Boolean expression with Excusive-NOR and NOR gates:
   $F = A\overline{B}C\overline{D} + \overline{A}BC\overline{D} + A\overline{B}\ \ \overline{C}D + \overline{A}B\overline{C}D$
   (b) If $F_1 = wx\overline{y}+\overline{y}\ \ \overline{z}+\overline{w}y\overline{z}+xy\overline{z}$ And $F_2 = (w + x + \overline{y} + \overline{z})\,(\overline{x} + \overline{y} + z)\,(\overline{w} + y + \overline{z})$ Obtain minterms list of $F_1 \bullet F_2$ using K-map obtain minimal SOP function of $F_1 \bullet F_2$. [8+8]

4. (a) A multiple output combinational logic circuit is defined by the following functions. Draw the schematic circuits for F_1 and F_2.
   $F_1(A, B, C, D) = \overline{\overline{A} \bullet \overline{\overline{A}D}} \bullet \left(\overline{A} + BC\right)$
   $F_2(A, B, C, D) = \overline{\overline{A}D} \bullet \left(\overline{A} + BC\right)$
   Using K-Maps simplify F_1 and F_2 and draw the reduced diagram circuit.
   (b) Design a full - subtractor circuit with three inputs x,y,z and outputs D, B. The circuit subtracts X - Y - Z where Z is the input borrow, B is the output borrow and D is the difference draw the circuit using NAND gates. [8+8]

Code No: X0524/R07 **Set No. 3**

5. (a) Define the following terms related to filp-flops.
   i. set-up time
   ii. hold time
   iii. propagation delay
   iv. preset and
   v. clear.
   (b) Distinguish between combinational logic and sequential logic. [10+6]

6. Design a circuit with three 4-bit registers A,B and C to perform the following operations.
   (a) Transfer two binary numbers to A and B when a start signal is enabled,
   (b) If A <B, shift left the contents of A and transfer the result to register C.
   (c) If A >B, shift right the contents of B and transfer the result to register C.
   (d) If A=B, transfer the number to register C unchanged.

   Explain the procedure. [16]

7. (a) What is parity checking? Explain its necessity and how is it implemented?
   (b) How many parity check bits must be included with the data word to achieve single error-connection and double-error detection when the data contains
   i. 16 bits
   ii. 32 bits
   iii. 48 bits. [8+8]

8. (a) Describe the operation of the SR Latch using NAND gate with the help of truth table, transition table and the circuit.
   (b) Explain the operation and use of De bounce circuit. [8+8]

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Code No: X0524/R07 **Set No. 4**

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1. (a) Generate Hamming code for the given 11 bit message 11001001100 and rewrite the entire message with Hamming code.
   (b) The binary numbers listed have a sign bit in the left most position and , if negative numbers are in 1's complement form. Perform the arithmetic operations indicated and verify the answers. [8+8]
      i. 101011 + 111001
      ii. 001111 + 110010
      iii. 111001 - 011010
      iv. 101111 - 100110.

2. (a) Express the following functions in sum of minterms and product of maxterms.
      i. F (A,B,C,D) = B'D + A'D + BD
      ii. F(x,y,z) = (xy + z)(xz + y).
   (b) Obtain the complement of the following Boolean expressions.
      i. (AB' + AC')(BC + BC')(ABC)
      ii. AB'C + A'BC + ABC
      iii. (ABC)'(A + B + C)'
      iv. A + B'C (A + B + C'). [8+8]

3. (a) With the use of map obtain minimal SOP expression for the function $F_3 = F_1 \bullet F_2$ Where F_1 and F_2 are shown below:
   $F_1 = AB\overline{C} + \overline{C}D + \overline{A}C\overline{D} + \overline{B}C\overline{D}$
   $F_2 = \left(A + B + \overline{C} + \overline{D}\right)\left(\overline{B} + \overline{C} + D\right)\left(\overline{A} + C + \overline{D}\right)$
   (b) Use K - map to obtain minimal SOP expression for the function given below and draw the circuit using NOR - gates.
   $F\left(A, B, C, D\right) = \overline{A}B\overline{C} + \overline{A}BC + AB\overline{C} + \overline{A}\ \overline{B}C + \overline{C}D + \overline{A}B + \overline{A}BC\overline{D}$

4. (a) Design a code converter to convert 8421 code to excess - 3 code.
   Consider all invalid combinations, as don't cares. Draw the circuit using only NAND gates.
   (b) A Boolean function is defined as follows. Draw schematic circuit for the given function F. Using K-map obtain its minimal SOP expression and draw the reduced diagram.$F = \left(A + \overline{B}C\right) + \left(\overline{A}B \oplus D\right)$ [8+8]

Code No: X0524/R07 **Set No. 4**

5. (a) Explain the following terms related to filp-flops.
   i. race round conditions
   ii. propagation delay
   iii. clock.
   (b) Explain the operation of R-S flip-flop with negative edge triggering with neat sketch. And explain its truth table. [8+8]

6. Draw the sequential circuit for serial adder using shift registers, full adder and D-FF. Explain its operation with state equations and state table . [16]

7. (a) Give the HDL code for a memory read, write operations if the memory size is 64 words of 4 bits each. Also explain the code.
   (b) A 16K * 4 memory uses coincident decoding by splitting the internal decoder into X-selection and Y-selection. [8+8]
   i. What is the size of each decoder and how many AND gates are required for decoding the address?
   ii. Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6,000.

8. (a) Describe the analysis procedure of asynchronous sequential logic using flow table.
   (b) Obtain a primitive flow table for a circuit with two inputs, x_1 and x_2 and two outputs z_1 and z_2, which satisfy the following four conditions:
   i. When $x_1x_2 = 00$, the output $z_1z_2 = 00$
   ii. When $x_1 = 1$ and x_2 changes from 0 to 1, the output is $z_1z_2 = 01$
   iii. When $x_2 = 1$ and x_1 changes from 0 to 1, the output is $z_1z_2 = 10$.
   iv. Otherwise, the output does not change. [6+10]

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