Code No: R21054 **R10** SET - 1

II B. Tech I Semester, Regular Examinations, Nov – 2012
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Construct a table for 4 -3 -2 -1 weighted code and write 9154 using this code
   b) Perform arithmetic operation indicated below. Follow signed bit notation:
      i) 001110 + 110010
      ii) 101011 - 100110.
   c) Explain the importance of gray code. (4M+8M+3M)

2. Convert each of the following to the other canonical form:
   a) F(x,y,z) = ∑(2,5,6)
   b) F(A,B,C,D) = π (0,1,2,4,7,9,12) (6M+9M)

3. Simplify the following functions by first finding the essential prime implicants
   i) F(w,x,y,z)= ∑(0,2,4,5,6,7,8,10,13,15)
   ii) F(w,x,y,z)= ∑(0,2,3,5,7,8,10,11,14,15) (7M+8M)

4. Design a full subtract or circuit with three inputs x, y, B_{in}, and two outputs D_{iff} and Bout. The circuits subtracts x-y- B_{in} , where Bin is the input barrow, B_{out} is the output borrow, and D_{iff} is the difference. (15M)

5. a) Implement the following functions on decoder logic
   Y1= Σ (0,1,3,6,7), Y2= Π (0,2,4,7), Y3= Π (1,3,6,7)
   b) Realize a full sub tractor using MUX. (7M+8M)

6. Implement the following functions on PLA
   A (w,x ,y,z) = Σ(0, 2, 6, 7, 8, 9, 12, 13)
   B (w,x ,y,z) = Σ(0, 2, 6, 7, 8, 9, 12, 13, 14)
   C (w,x ,y,z) = Σ(2, 3, 8, 9, 10, 12, 13)
   D (w,x ,y,z) = Σ(1, 3, 4, 6, 9, 12, 14) (15M)

7. a) Define the following terms related to flip-flops.
      i) set-up time ii) hold time iii) propagation delay iv) preset and v) clear.
   b) Distinguish between combinational logic and sequential logic. (9M+6M)

8. Explain about the Following
   a) Serial addition in 4-bit shift register
   b) BCD Ripple Counter
   c) Universal Shift Register. (5M+5M+5M)
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Code No: R21054 **R10** SET - 2

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1. Express the following numbers in decimal:
   a) $\{10110.0101)_2$ b) $(l6.5)_{16}$
   c) $(26.24)_8$ d) $(FAFA)_{16}$
   e) $(1010.1010)_2$ (15M)

2. Implement the Boolean function
   F = xy + x'y' + y'
   a) With AND and inverter gates,
   b) With NAND and inverter gates,. and
   c) With NOR and inverter gates. (5M+5M+5M)

3. Simplify the following Boolean functions, using four variable maps:
   a) F(w, x, y, z) = ∑(1,4,5,6,12,14,15)
   b) F(A,B,C,D) = ∑(1,5,9,10,11,14,15)
   c) F(w, x,y,z) =∑ (0,1,4.5,6,7,8,9) (5M+6M+4M)

4. a) Design a 4 bit carry look ahead adder circuit.
   b) Design a 4 bit BCD adder using Full adder circuits (7M+8M)

5. a) Design a 2 bit comparator using gates.
   b) Implement the following functions on decoder logic
   i) Y1= Σ (0,1,3,6,7), Y2= Π (0,2,4,7), ii) Y3= Π (1,3,6,7) (6M+9M)

6. Tabulate the truth table for an 8 × 4 ROM to implement the following Boolean expression.
   A(x,y,z)= ∑ (3,6,7) B(x,y,z)= ∑ (0,1,4)
   C(x,y,z)= ∑ (2,6) D(x,y,z)= ∑ (0,2,5,6) (4M+4M+4M+3M)

7. Explain the design of Sequential circuit with an example. Show the state reduction, state assignment. (15M)

8. a) Draw and explain 4-bit universal shift register.
   b) Explain different types of shift registers. (7M+8M)
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Code No: R21054 **R10** SET - 3

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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
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1. a) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend:
   i) 100 – 110000 ii) 11010 - 1101.
   b) Construct a table for 4 -3 -2 -1 weighted code and write 9154 using this code
   c) Perform arithmetic operation indicated below. Follow signed bit notation:
   i) 001110 + 110010 ii) 101011 - 100110.
   d) Explain the importance of gray code. (4M+4M+4M+3M)

2. Draw logic diagrams to implement the following Boolean expressions
   a) Y = A + B + B'(A + C') b) Y = A(B EX-OR D) + C'
   c) Y = (A' + B') (C + D') d) Y = [(A + B') (C' + D)] (4M+4M+4M+3M)

3. Implement the following Boolean function F, using the two-level form logic
   a) NAND-AND, b) AND-NOR, c) OR-NAND
   F(A,B,C,D)= ∑ (0,4,8,9,10,11,12,14) (15M)

4. a) Implement Half adder using 5 NAND gates
   b) Implement full subtractor using NAND gates only. (5M+10M)

5. a) Implement a 64 :1 MUX using 16:1 and 4:1 Muxs.
   b) Realize a BCD to Excees-3 code converter using MUX. (7M+8M)

6. Tabulate the truth table for 8 x 4 ROM to input the following functions:
   i) A= Σ (1,2,4,6) ii) B=Σ(0,1,6,7) iii) C= Σ (2,6) iv)D=Σ(1,2,3,5,7) (15M)

7. a) Convert a T flip flop to D type flip flop
   b) Determine how the circuit shown in Fig. 7.12 functions as a T-type flip-flop.
   What problem would there be when T= 1 and how could it be resolved.

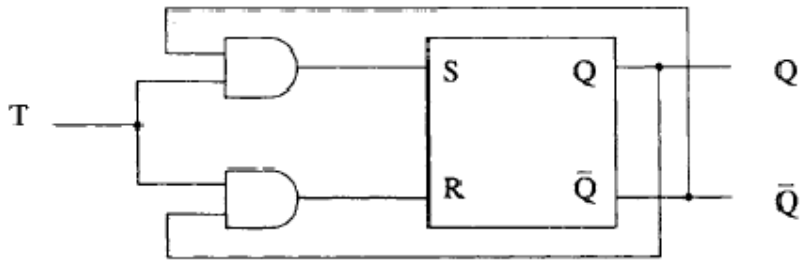

Fig. 7.12

(7M+8M)

8. Define BCD Counter and Draw its State table? (15M)
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Code No: R21054 **R10** SET - 4

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1. a) What is ABE_H, in decimal?
   b) Perform 64_{10}- 83_{10} using ten's complement arithmetic.
   c) What is 100111110011_2 in hexadecimal?
   d) Subtract-5 from-8 using binary notation. (4M+4M+4M+3M)

2. a) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa
   b) Convert each of the following expressions into sum of products and product of sum:
   i) (AB + C)(B + C'D) ii) x' + x(x + y')(y + z') (7M+8M)

3. Simplify the follow Boolean functions, using four variable maps:
   a) F(w,x, y,z) = ∑(1,4,5,6,12,14,15)
   b)F(A,B,C, D) = ∑ (1,5,9,10,11,14,15) (7M+8M)

4. a) Design a 4 bit carry look ahead adder circuit.
   b) Implement full subtractor using NAND gates only. (7M+8M)

5. a) Design a BCD to Gray code converter using 8:1 MUXS.
   b) Write a HDL program to model an 8 bit comparator using 2 bit comparators. (7M+8M)

6. a) How many 32kX8 RAM chips are needed to provide a memory capacity of 256k bytes?
   b) How many lines of address must be used to access 256kbytes? How many of these lines are connected to the address inputs of all chips?
   c) How many lines must be decoded for the chip select inputs ?specify the size of decoder. (15M)

7. a) How many flip-flops are required to construct mod-12 ring and Johnson counters?
   b) How could:
   i) a JK flip-flop be used as a D-type?
   ii) a JK flip-flop be used as a T-type?
   iii) a D-type flip-flop be used as a T-type? (6M+9M)

8. Design a left shift and right shift for the following data
   10110101 (15M)
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