

Code No: X0425

R07**SET - 1****II B. Tech I Semester Supplementary Examinations May – 2013****ELECTRONIC CIRCUIT ANALYSIS**

(Electronics and Communications Engineering)

Time: 3 hours

Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks

1. a) Draw the circuit diagram and low frequency equivalent circuit of common source amplifier and derive an expression for its voltage gain.
b) For the emitter follower circuit with $R_S = 0.5K$ and $R_L = 5K$, calculate A_I , R_i , A_V , A_{V_S} , and R_o . Assume, $h_{fe} = 50$, $h_{ie} = 1K$, $h_{oe} = 25 \mu A/V$.
2. a) A two stage amplifier (CE-CC configuration) is shown in the below Figure 1. The h parameter values are $h_{fe}=50$, $h_{ie}=2k\Omega$, $h_{re}=6 \times 10^{-4}$, $h_{oe}=25 \mu A/V$, $h_{fc}=-51$, $h_{ic}=2k\Omega$, $h_{rc}=1$, $h_{oc}=25 \mu A/V$. Find the input and output impedances as well as overall voltage and current gains.

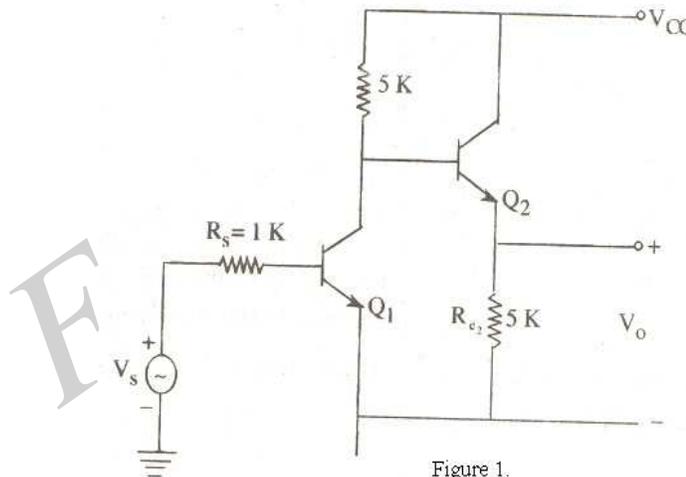


Figure 1.

- b) Draw the circuit diagram of Darlington pair circuit deriving its important characteristics?
3. a) Derive the expression of CE short circuit current gain A_I as function of frequency using hybrid π model.
b) What is the relationship between f_T and f_β ? Discuss the significance of f_T ?

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4. a) A single transistor is operating as an ideal class-B amplifier with a 500Ω load. A D.C meter in the collector circuit reads 10mA. How much signal power is delivered to the load?
b) Show that the even harmonics are eliminated in Class B push pull configuration?
5. a) Explain various neutralization techniques in tuned amplifiers with the help of circuit diagrams?
b) Mention the three methods of stabilization of a single tuned BJT amplifier?
6. a) In class B amplifier $V_{ce(\min)}=2V$ and supply voltage $V_{cc}=15V$. Find collector circuit efficiency?
b) Explain the reasons for oscillation in a tuned amplifier. Briefly explain the methods used to stabilize the tuned amplifiers against oscillations?
7. a) Explain the operations of
 - i) Half wave voltage doubler circuit
 - ii) Full wave voltage regulatorb) Draw and explain the load voltage and current characteristic for a current limited regulator?
8. a) Draw the block diagram of SMPS and explain its working with the help of waveforms?
b) Explain how three terminal IC 7805 is used as a current source with a neat circuit diagram?

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R07**SET - 2****II B. Tech I Semester Supplementary Examinations May – 2013****ELECTRONIC CIRCUIT ANALYSIS**

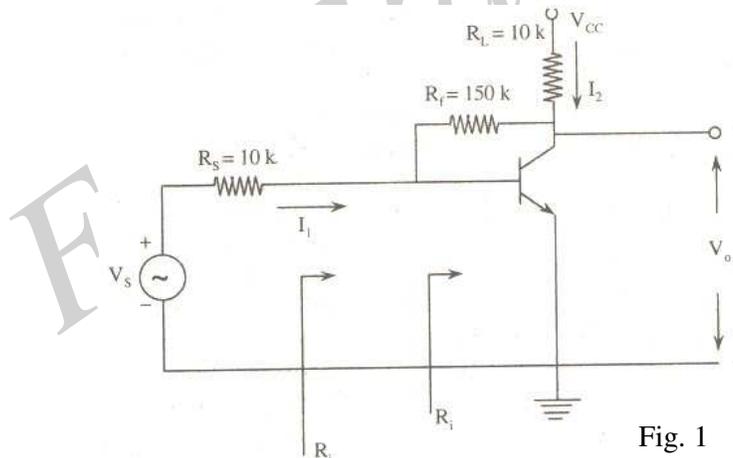
(Electronics and Communications Engineering)

Time: 3 hours

Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks

1. a) In a single stage CB amplifier circuit $R_e=20k$, $R_c=10k$, $V_{EE}=-20V$, $V_{CC}=20V$, $R_L=10k$ and $R_s=0.5k$ Find A_i , R_i , R_o , A_v
- b) Draw the basic circuit of CS amplifier with load Resistor R_d in drain circuit and an additional Resistor R_s in the source to ground circuit?
2. a) Three identical non interacting amplifier stages in cascade have an overall gain of 1dB down to 30 compared to mid-band. Calculate the lower cutoff frequency of the individual stages?
- b) For the amplifier shown in fig. 1, calculate R_i , R_i^1 , A_v , A_{v_s} and $A_f=-I_2/I_1$. The h-parameter values are $h_{fe}=50$, $h_{ie}=1.1k\Omega$, $h_{re}=2.5 \times 10^{-4}$, $h_{oc}=24\mu A/V$.



3. a) In a hybrid π model of a transistor at high frequencies, how does C_c vary with $|I_c|$ and $|V_{CE}|$?
How does C_c vary with $|I_c|$ and $|V_{CE}|$?
- b) A single stage CE amplifier is measured to have a voltage gain bandwidth f_H of 5MHz with $R_L=500\Omega$. Assume $h_{fe}=100$, $g_m=100mA/V$, $r_{bb1}=100\Omega$, $C_c=1pF$ and $f_T=400MHz$. Find the value of source Resistance that will give the required bandwidth?

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4. a) Explain about different types of distortions that occur in amplifier circuits?
b) Define the conversion efficiency of power amplifier. A class A power amplifier with direct coupled load has a collector efficiency of 15% and delivers a power output of 5 watts. Find
 - i) The dc power input?
 - ii) Power dissipation at maximum output?

5. a) Draw the circuit diagram and small signal A.C equivalent circuit of a single tuned amplifier with the tank circuit connected at the input side?
b) Derive the equation for the 3db band width capacitance coupled single tuned amplifiers?

6. a) Explain as to how you can increase the selectivity of single tuned amplifiers. Draw the circuit diagram and explain its operation and also draw its frequency response?
b) A constant generator drives a parallel tuned circuit consisting of a lossless capacitor 'C' and A coil 'L' (having small resistance 'R'). Derive the expression for the frequency of resonance?

7. a) Draw and explain a circuit which limits the current that can be drawn from the supply to a certain specific maximum?
b) Draw and explain the regulator which will provide the fold back limiting?

8. a) Explain different types of protections required in IC Voltage regulators?
b) Explain the operation of basic switching type regulator with a circuit diagram?

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R07**SET - 3****II B. Tech I Semester Supplementary Examinations May – 2013****ELECTRONIC CIRCUIT ANALYSIS**

(Electronics and Communications Engineering)

Time: 3 hours

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1. a) Draw the basic circuit of common gate amplifier Find  $R_i$ ,  $R_o$  and gain ?  
b) For a CE configuration, what is the maximum value of  $R_S$  for which  $R_o$  differs by no more than 10 percent of its value for  $R_S = 0$ . The h-parameter values are  $h_{fe} = 50$ ,  $h_{ie} = 1.1K$ ,  $h_{re} = 2.5 \times 10^{-4}$ ,  $h_{oe} = 25 \mu A/V$ .
2. a) A two stage FET RC Coupled amplifier has the following parameters  $G_m = 10mA/V$ ,  $r_d = 5.5k$  and  $R_g = 0.5M$  for each stage. Assume  $C_s$  is large
  - i) What must be the value of  $C_b$  in order that the frequency characteristics of each stage be flat within 1 db down to 10 Hz?
  - ii) Repeat the above part if the overall gain of both stages is to be down 1 db at 10 Hz?
  - iii) What is the overall mid band voltage gain?
 b) Derive the expression of the high 3db frequency  $f_H^*$  of n identical non interacting stages in terms of  $f_H$  for one stage?
3. a) Draw the circuit of Class A series fed amplifier and derive the expression for output power?  
b) A single transistor is operating as an ideal class-B amplifier with a  $500\Omega$  load. A D.C meter in the collector circuit reads 10mA. How much signal power is delivered to the load?
4. a) Draw the circuit diagram of a complementary symmetry push pull amplifier and explain its Working?  
b) A transistor in a transformer coupled Class –A power amplifier has to deliver a maximum of 5 watts to a load of  $4\Omega$  load. The quiescent point is adjusted for symmetrical swing and the collector supply voltage is  $V_{cc} = 20V$ . Assume  $V_{min} = 0V$ 
  - i) What is the transformer turns ratio?      ii) What is the peak collector current?
 c) What is cross over distortion? How can a class AB power amplifier avoid cross over distortion?

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5. a) Explain in detail how do you alter the bandwidth of an RF amplifier which is  
i) Single tuned          ii) Double tuned  
b) Draw the high frequency equivalent circuit of a Tapped Single tuned capacitance coupled Amplifier using BJT and derive the expression for i) Voltage gain ii) Gain at Resonance
6. a) Explain in detail the effect of cascading tuned amplifier and hence derive the expression for bandwidth of n-stage amplifier. Also draw the frequency response and explain what happens as the number of stages increases?  
b) What are the main advantages of class-C operating mode in RF applications?
7. a) A power supply having output resistance of  $2\Omega$  supplies a full load current of 100mA to a  $50\Omega$  load. Find the percentage voltage regulations and no load output voltage of the supply?  
b) Explain why voltage regulators are called as closed loop control systems?
8. a) Why switching frequencies are limited in switching regulator and also explain how to overcome this?  
b) What is voltage multiplier? Draw and explain the circuit of it and give its applications?

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**R07****SET - 4****II B. Tech I Semester Supplementary Examinations May – 2013****ELECTRONIC CIRCUIT ANALYSIS**

(Electronics and Communications Engineering)

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1. a) For a CE configuration what is the maximum value of  $R_s$  for which  $R_o$  differs by no more than 50% of its value for  $R_s=0$ ? The h parameter values are  $h_{fe}=50, h_{ie}=1.1k\Omega, h_{re}=2.5 \times 10^{-4}, h_{oe}=25\mu A/V$
- b) For CD amplifier as shown in Figure 1,  $G_m=3.5ms, r_d=25k\Omega$ , Calculate  $R_i, R_o$  and  $A_v$

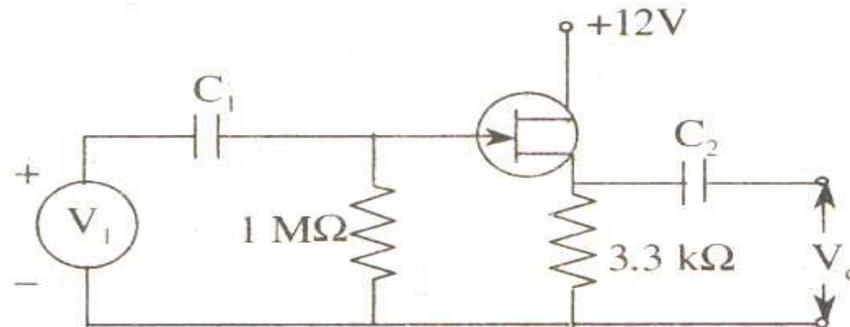


Figure 1.

2. a) Draw the circuit of two stage RC Coupled JFET amplifier and explain its working?
- b) A two stage FET RC coupled amplifier has the following parameters  $g_m=10mA/V, r_d=5.5k$  and  $R_g=0.5M$  for each stage. Assume  $C_s$  is large calculate  $R_i, A_{vs}$ .
3. a) Given the following transistor measurements made at  $I_c=5mA, V_{ce}=10V$  and at room temperature  $h_{fe}=100, h_{ie}=600$  and  $A_f=10$  at 10MHz,  $C_c=3pf$ . Find  $f_\beta, f_T, C_e, r_{b1e}$  and  $r_{bb1}$ ?
- b) Draw the small signal equivalent circuit for an emitter follower stage at high frequencies and explain the working of it?
4. a) Draw the push pull power amplifier circuit. Derive the expression for the out put current in push pull amplifier with base current as  $I_b=I_{bn} \sin\omega t$ ?
- b) In transformer coupled class A power amplifier show that the conversion efficiency is 50%?

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5. a) Draw Single tuned inductively coupled BJT high frequency circuit and explain it?  
b) Explain in detail the need for tapped inductance in tuned amplifiers?
  
6. a) Draw the circuit of class-C radio frequency amplifier and explain its operation with necessary waveforms?  
b) Explain the principle of a wideband amplifier?
  
7. a) With the help of a neat circuit diagram, explain the operation of BJT shunt voltage regulator?  
b) A power supply having output resistance of 2 ohms supplies a full load current of 100mA to a 50 ohms load. Find the percent voltage regulations and no load output voltage of the supply?
  
8. a) Explain how three terminal IC 7805 is used as current source with a neat diagram?  
b) What are the limitations and important features of three terminal regulators?