Code No: X0223 **R07** SET - 1

II B. Tech I Semester, Supplementary Examinations, Nov – 2012
PULSE AND DIGITAL CIRCUITS
(Com. to EEE, EIE)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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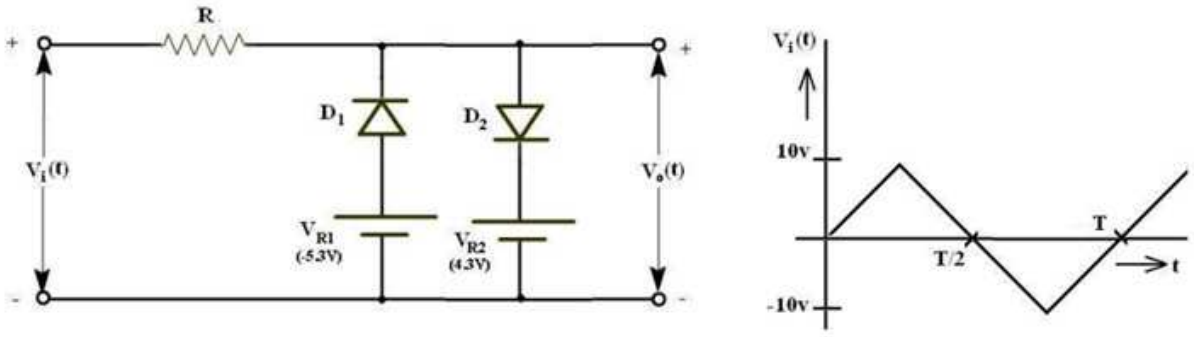
1. a) Define the rise time and derive an expression for the rise time of the output of a low-pass circuit excited by a step input.
   b) An ideal 1 millisecond pulse is fed to a low-pass circuit. Calculate and plot the output waveform under the following conditions. The upper 3-dB frequency is
   i)10 MHz, ii) 1MHz, iii) 0.1 MHz.

2. a) Determine the output waveform of the two-level diode clipping circuit shown for the triangular input. (V_{R1} = -5.3V; V_{R2} = 4.3V)



   b) Explain the term 'biased clamping'. A 100V peak square wave with an average value of 0V and a period of 20ms is to be negatively clamped at 25V. Draw the input and output waveforms and necessary circuit diagram.

3. a) Describe how a transistor functions as a switch in the CE configuration in ON state and in OFF state.
   b) Explain storage and transition times of the diode as a switch.

4. Draw the circuit diagram and explain the working of an Astable multivibrator with the relevant waveforms. Derive an expression for the frequency of oscillations. Show that it can be used as a voltage to frequency converter.
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5. a) With the help of a neat circuit diagram and waveforms, explain the working of a transistor bootstrap time base generator.
   b) Compare the Miller and Bootstrap circuits.

6. Explain the following
   a) Synchronization of a sweep generator with pulse signals.
   b) Sine wave frequency division with a sweep circuit.

7. a) How do the sampling gates different from logic gates? Draw the circuit diagram of unidirectional sampling gate and explain its working. Also explain how the loading of the control signal is reduced when the number of input increases.
   b) What are the advantages and disadvantages of the unidirectional diode gate?

8. a) Define the terms 'Fan-in' and 'Fan-out'. Explain the DTL NAND gate circuit which can improve Fan out of the gate.
   b) Give the comparison between various logic families.

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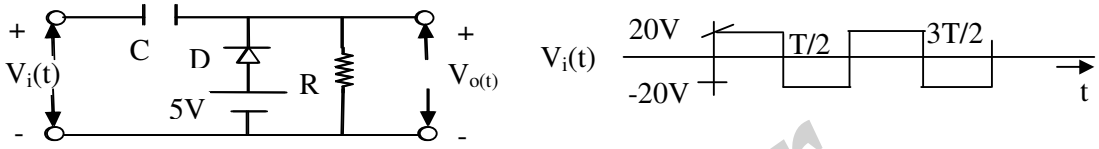
1. a) Draw the high-pass circuit and explain its working.
   b) Derive an expression for the output of a high-pass circuit excited by an exponential input.

2. a) With the help of a neat circuit diagram, explain the working of an emitter-coupled clipper.
   b) Determine the output waveform of the clamping circuit for the square wave input.



3. a) Draw the collector waveform of transistor switch and indicate all the time intervals. What are the factors that contribute the delay time of transistor switch? Define the storage time constant and how it is related to storage time of transistor switch?
   b) Explain the variation of saturation parameters of transistor with temperature.

4. a) With the help of a neat circuit diagram explain the working of a fixed –bias bistable multivibrator. Derive the expression for the resolution time and maximum switching speed of a bistable multivibrator.
   b) With the help of a suitable circuit diagram, explain the methods of symmetric and un symmetric triggering of a bistable multivibrator.

5. a) Define slope, transmission and displacement errors and derive the relation between them.
   b) Draw and explain working of voltage time base generator by clearly indicating the sweep time and restoration time on the typical waveform.

6. a) What is the condition to be met from pulse synchronization of monostable circuits? Explain the use of monostable relaxation device as a divider.
   b) What is phase jitter? How to reduce it in frequency division?

7. a) Compare unidirectional and bidirectional sampling gates.
   b) Sketch circuit of a simple diode bi-directional sampling gate and describe its functioning with neat waveforms. Also sketch the circuit in the form of a bridge and obtain expressions for gain A and the two minimum control voltage levels $(V_C)_{min}$ $(V_n)_{min}$.

8. a) With the help of neat circuit diagram and truth table, explain the working of three input DTL NAND gate.
   b) Write the following a) DTL NAND gate, b) RTL NOR gate. c) Prove that NAND and NOR gates are universal gates.
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Code No: X0223 **R07** SET - 3

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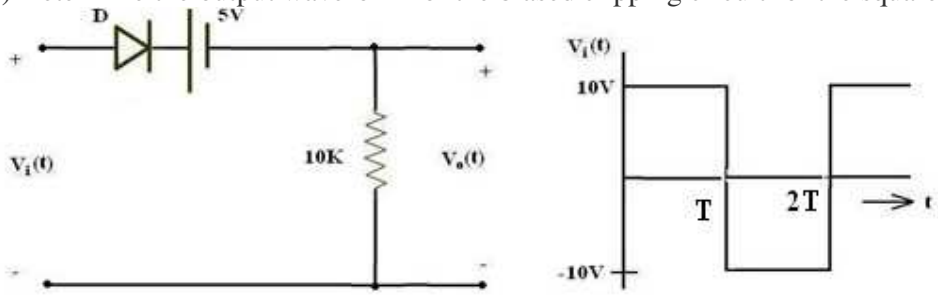
1. a) Derive an expression for percentage tilt of the output of a high pass circuit with large time constant excited by a symmetrical square wave with zero average value.
   b) Draw and explain the response of RLC circuit for a step input.

2. a) What is clamper? How it is used in Non-linear wave shaping?
   b) Determine the output waveform for the biased clipping circuit for the square wave input.



3. a) Define and derive the expressions for the rise time and fall time of a transistor switch.
   b) Consider a transistor switch in CE configuration operating with V_{CC} =18 V and V_{BB} = 0 V. The collector resistance R_C = 3.9 kΩ and R_2 = 3 R_1. Assume that V_{BE} (sat) = 0 V and V_{CE} (sat) = 0 V. The static current gain h_{FE} of the transistor is 50. Determine the minimum value of I_B to keep the transistor in saturation when it is in its ON state?

4. a) Explain the working of a Schmitt trigger with the help of neat circuit diagram and waveforms. Define the terms upper triggering point and lower triggering point.
   b) Explain how Schmitt trigger act as a comparator.

5. a) Draw and explain the operation of a constant current sweep circuit and derive the expression for sweep voltage.
   b) How the linearity can be corrected through the adjustment of driving waveform.

6. a) Mention the principle involved in the synchronization of voltage sweep waveform with a sinusoidal synchronization signal.
   b) Describe synchronization with 2:1 frequency division with neat waveforms.

7. a) Sketch and explain the operation of a simple diode unidirectional sampling gate whose output is not affected by the higher voltage level – V_2 of the control input.
   b) Explain how a sampling gate is used in chopper amplifier?

8. a) Explain the operation of a two input TTL logic gate with open collector configuration. What are the applications of open collector gates?
   b) Define positive and negative logic systems.
   c) Draw a diode AND circuit for negative logic and explain how it works.
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1. a) Prove that an RC circuit behaves as a reasonably good integrator if RC> 15 T, where T is the period of an input 'Em sin ωt'.
   b) A 12 Hz symmetrical square wave whose peak-to-peak amplitude is 5 V is impressed upon a high-pass circuit whose lower 3 dB frequency is 15 Hz. Determine the peak-to- peak amplitude of the output waveform. Determine the corner voltages of the output waveform. Also sketch the input waveform and the output waveform to the same scale.

2. a) State and prove the clamping circuit theorem
   b) Draw a circuit to transmit that part of a sine wave which lies -3V and +6V and explain its working.

3. a) Describe the switching times of BJT by considering the charge distribution across the base region. Explain this for cut off, active and saturation regions.
   b) How does the temperature affect the saturation junction voltages of a transistor?

4. a) With the help of neat circuit diagram explain the working of a collector coupled Monostable Multivibrator. Derive an expression for the gate width of monostable multivibrator.
   b) Realize A collector –coupled monostable multivibrator using two *n-p-n* silicon transistors with the following parameters – V_{CC} = 20 V, V_{BB} = 8 V, R_C = 3.9 kΩ , R1 = R2 = R = 39 kΩ, h_{FE} = 30, $r_{bb'}$ =200 Ω and C = 620 pF. Determine the pulse width of the output waveform. The reverse saturation current ICBO may be neglected.

5. a) Illustrate the method of generation of a current sweep waveform with the help of a single transistor current sweep circuit. Sketch the gating waveform, the current sweep wave form, and the collector waveform.
   b) Obtain an expression for slope error in a current sweep circuit employing a practical yoke. Simplify this expression. Also derive an expression for sweep-speed mathematically.

6. a) Define the terms phase delay and phase jitter.
   b) Describe the pulse synchronization of an astable relaxation circuit with neat waveforms.

7. Why are sampling gates called Selection circuits? Write some applications of sampling gates. Describe the operation of the four-diode sampling gates.

8. a) Draw and explain the circuit diagram of integrated positive RTL NOR gate.
   b) Compare the RTL and DTL logic families in terms of Fan out, propagation delay, power dissipated per gate and noise immunity.
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