Code No: X0224 **R07** SET - 1

II B. Tech I Semester Supplementary Examinations May – 2013
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, EIE, BME, ECC)

Time: 3 hours Max. Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) How to convert a gray number to binary? Explain with the help of suitable examples?
   b) Perform the following binary subtraction:
      i) 1011-101 ii) 10110-1011 iii) 1100.10-111.01 iv) 10001.01-1111.11
   c) Convert the following numbers into the gray numbers
      i) $3A7_{16}$ ii) 527_8 iii) 652_{10}

2. a) Name the gates that are used as universal gates? Explain?
   b) Realize the following function as i) Multilevel NAND-NAND gate network ii) Multilevel NOR-NOR network.
      $f = B(A + CD) + A\overline{C}$

3. a) Simplify the Boolean function using SOP.
      i) $f(A, B, C, D) = \sum(0, 1, 2, 5, 8, 9, 10)$
      ii) $f(A, B, C, D) = \sum(0, 1, 2, 3, 7, 8, 9, 10, 11, 12, 13)$
   b) Reduce the following expressions using K-maps
      i) $AB + A\overline{B}C + \overline{A}B\overline{C} + B\overline{C}$
      ii) $AB\overline{C} + AB + C + B\overline{C} + D\overline{B}$

4. a) Design a 32:1multiplexer using two 16:1 and 2:1multiplexers.
   b) Realize the logic expressions given below using a
      i) 8:1 MUX ii) 16:1 MUX
      $F = \sum_m(0, 1, 3, 5, 8, 11, 12, 14, 15)$

5. a) Compare the three combinational PLDs-PROM, PLA and PAL.
   b) Tabulate the PLA programming table for the four Boolean functions listed below
      A(x,y,z) = ε (1, 2, 4, 6)
      B(x,y,z) = ε (0, 1, 6, 7)
      C(x,y,z) = ε (2,6)
      D(x,y,z) = ε (1, 2, 3, 5, 7)
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6. a) Distinguish between combinational and sequential switching circuits?
   b) What are the various methods used for triggering a flip-flop?
   c) Design a sequence detector which generates an output z=1, whenever the string is 0110 and generates a 0 at all other times. The overlapping sequences are detected. Implement the circuit using D flip flops.

7. a) Compare and contrast the Moore machine and the Melay machine.
   b) Obtain the set of maximal compatibles for the sequential machine whose state table is shown in the following table, by using the merger table method.

PS	NS, Z			
	I_1	I_2	I_3	I_4
A	-	C,1	E,1	B,1
B	E,0	-	-	-
C	F,0	F,1	-	-
D	-	-	B,1	-
E	-	F,1	A,0	D,1
F	C,0	-	B,0	C,1

8. Obtain the ASM chart for the following state transitions:
   a) If x=0, control goes from state T_1 to state T_2. If x=1, generate the conditional operation and go from T_1 to T_2.
   b) If x=1, control goes from T_1 to T_2 and then to T_3. If x=0, control goes from T_1 to T_3

Code No: X0224 **R07** SET - 2

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1. a) What do you mean by an error correcting code?
   b) Perform the following subtractions in excess-3 code using the 9's complement method.
      i) 687-348 ii) 246-592
   c) Convert the following numbers with the given radix to decimal and binary.
      i) 4433_5 ii) 1199_{12} iii) 5654_7

2. a) Explain how the basic gates can be realized using NAND gates.
   b) Realize i) $Y = A + BC\overline{D}$ using NAND gates and ii) $Y = (A + C)(A + \overline{D})(A + B + \overline{C})$ using NOR gates.
   c) Reduce the following Boolean expressions
      i) $AB + BB + C + \overline{B}$ ii) $(AB + C)(AB + D)$

3. Obtain the minimal expression using the tabular method and implement it in universal logic.
   $\sum_m (1, 5, 6, 12, 13, 14) + d(2, 4)$

4. a) Design a circuit to covert excess-3 code into BCD code using a 4 bit full adder.
   b) Implement the function $F(a, b, c, d) = a\overline{b} + acd + b\overline{c} + d$ using a MUX with 3 select inputs.

5. Write a short note on the following
   a) Architecture of PLDs
   b) Capabilities and limitations of threshold gates

6. a) Define the following terms with relation to flip-flops
      i) Set-up time ii) hold time iii) propagation delay time
      iv) Preset v) clear.
   b) Draw the circuit diagram of 4-bit ring counter using D-flip flops and explain its operation With the help of bit pattern.
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7. a) Explain the limitations of finite state machines.
   b) Find the equivalence partition and a corresponding reduced machine in standard form for the machine given in table

PS	NS,Z	
	X=0	X=1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

8. a) List out the salient features of ASM charts.
   b) Draw the ASM chart for the following state transition, start from the initial state T_1, then if xy=00 go to T_2, if xy=01 go to T_3, if xy=10 go to T_1, otherwise go to T_3 and design its control circuit using D-flip flop and decoder.

Code No: X0224 **R07** SET - 3

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1. a) What is the Hamming code? How is the Hamming code word tested and corrected?
   b) Explain binary subtraction using the 1's and 2's complement methods.
   c) Convert the following decimal numbers to octal numbers and then decimal to binary.
      i) 59 ii) 64.5 iii) 199.3

2. a) What do you mean by the principle of duality? List out the properties of Boolean algebra.
   b) Simplify the following expressions
      i) $\overline{A}B + C\overline{D}$ ii) $AB + \overline{AC} + A\overline{B}C(AB + C)$ iii) $(\overline{A} + B)(A + B)$
      iv) $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + AB\overline{C}$)

3. a) Simplify the Boolean function using SOP.
      i) $f(A, B, C, D) = \sum(1, 3, 7, 11, 15) + \sum_d(0, 2, 5)$
      ii) $f(A, B, C, D) = \sum(1, 2, 5, 6, 9) + \sum_d(10, 11, 12, 13, 14, 15)$
   b) Reduce the following expressions using K-maps
      i) $(A + B)(A + \overline{B} + C)(A + \overline{C})$ ii) $(\overline{A} + B)(A + B + \overline{D})(B + \overline{C})(B + CD)$

4. a) Show how a 16:1 MUX can be realized using 4:1 MUX.
   b) Implement the following logic function using an 8:1 MUX
      $F(a, b, c, d) = \bar{a}\,b + \bar{c}\,d + a\bar{c}$

5. a) Derive the PLA programming table for the combinational circuit that squares a 3 bit number.
   b) For the given 3-input, 4-output truth table of a combinations circuit, tabulate the PAL programming table for the circuit.

Inputs			Output			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1
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6. a) What is serial binary adder? Explain its working with the help of a state diagram.
   b) Design a Mod-6 synchronous counter using J-K flip flops.

7. a) Distinguish between Mealy and Moore machines
   b) Convert the following Mealy machine into a corresponding Moore machine

PS	NS,Z	
	X-0	X=1
A	B,0	E,0
B	E,0	D,0
C	D,1	A,0
D	C,1	E,0
E	B,0	D,0

8. a) Draw and explain the ASM chart for a weighing machine.
   b) Show the exit paths in an ASM block for all binary combinations of control variables x, y and z, starting from an initial state.

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1. a) List the salient features of the BCD, Excess-3 and Gray codes.
   b) How do you add two decimal numbers in the BCD form if the sum is greater than 9?
   c) Multiply the following binary numbers
      i) 1011 and 1101 ii) 100110 and 1001 iii) 1.01 and 10.1

2. a) obtain the duals of the following functions
      i) $\overline{A}B + \overline{A}B\overline{C} + \overline{A}BCD + \overline{A}B\overline{C}\overline{D}E$ ii) $ABEF + AB\overline{E}\overline{F} + \overline{A}\overline{B}EF$
      iii) $\overline{X}Z + \overline{X}Y + X\overline{Y}Z + YZ$ iv) $AB + \overline{AC} + A\overline{B}C$
   b) Reduce the following Boolean expressions
      i) $AB + A(B + C) + \overline{B}(B + D)$ ii) $(X + Y + Z)(\overline{X} + \overline{Y} + \overline{Z})X$
      iii) $A + B + \overline{A}\overline{B}C$ iv) $X(YZ + \overline{Y}Z)$

3. Obtain the minimal expression using the tabular method and implement it in universal logic.
   $\prod_M (1, 5, 6, 7, 11, 12, 13, 15)$

4. a) Write about the hazards and hazard free realizations.
   b) Design binary to gray code converter.

5. Find the function f(x_1, x_2, x_3, x_4) realized by each of the threshold networks shown in the figure: 5(a) i, 5(a)ii, 5b.

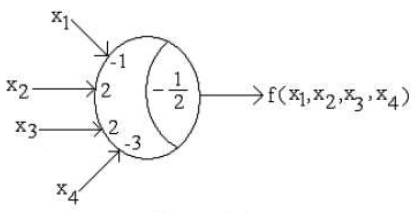

Figure 5(a)i

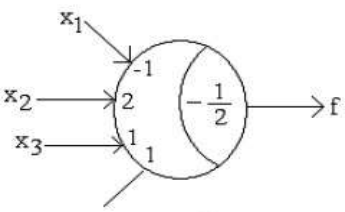

Figure 5(a)ii

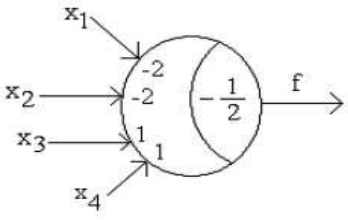

Figure 5b
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Code No: X0224 **R07** SET - 4

6. a) Explain the following
   i) Race around condition in J-K flip flop
   ii) Excitation table for flip-flops.
   b) Give the design of 4 bit Ring counter and explain with the help of waveforms. Also give the application of this ring counter.

7. What are the conditions for the two machines to be equivalent? For the machine given below, find the equivalence partition and a corresponding reduced machine in standard form:

PS	NS,Z	
	X=0	X=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

8. a) Draw and explain the ASM chart for a binary multiplier.
   b) Draw an ASM chart, a state diagram for the synchronous circuit having the following description. The circuit has a control input C, clock and outputs x,y,z.
   i) If C=1, on every clock rising edge, the code on the output x, y, z changes from 000→010→100→110→000 and repeats.
   ii) If C=0, the circuit holds the present state.