Roll No. | | | | | | | | | | | | |

Total No. of Pages : 02

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B.Sc. (CS) (2013 & Onwards) (Sem.–2)

COMPUTER SYSTEM ARCHITECTURE

Subject Code : BCS-206

M.Code : 71511

Time : 3 Hrs. Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains SIX questions carrying TEN marks each and a student has to attempt any FOUR questions.**

SECTION-A

1. Answer briefly :

a. What is the use of EEPROM?

b. What are shift micro-operations?

c. What is control bus?

d. Which registers are involved in fetch phase of instruction cycle?

e. Given examples of MIMD computers.

f. Differentiate between memory mapped I/O and isolated I/O.

g. What is the difference between selective set and selective complement logical micro operations?

h. What is handshaking?

i. What is the need of I/O interface unit?

j. What is the role of valid bit in cache initialization?

SECTION-B

2. Discuss 16 bit common bus system with neat diagram.

3. Write a short note on :

   a) Windows lite mobile device architecture.

   b) Set-Associative mapping.

4. What are addressing modes? Explain the various addressing modes with examples.

5. How data transfers can be controlled using handshaking technique?

6. a) Discuss stack organization of CPU. Also discuss Push and Pop operations of stack.

   b) How RAM and ROM chips are connected to CPU trough data and address buses?

7. Design a four bit combinational shifter to perform shift micro operations.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.