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17EC34

Third Semester B.E. Degree Examination, Dec.2019/Jin.2020
Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Express the following functions into a canonical form:
 0 $f_1 = a + be + bcd$
 ii) $f_2 = a(b + c)(b + c + d)$ (08 Marks)
 b. Represent the number of days in a month for a non-leap year by a truth cable, indicating the output of a invalid inputs if any by '0'. (06 Marks)
 c. Simplify the given function using K-map method
 $f(abcd) = \sum m(1, 2, 4, 11, 13, 14, 15) + d(0, 5, 7, 8, 10)$. (06 Marks)

OR

- 2 a. Find all prime implicants of the function using Quine-industry method and verify the same by K-map method. $f(abcd) = \sum m(0, 2, 3, 4, 8, 10, 12, 13, 14)$ (10 Marks)
 b. Find minimal sum and minimal product for the incomplete Boolean function using K-map
 $f(abcd) = \sum m(6, 7, 9, 10, 13) + d(1, 4, 5, 11, 15)$. (10 Marks)

Module-2

- 3 a. Design two bit magnitude comparator. (10 Marks)
 b. Design 4:2 priority encoder with a valid output where highest priority is given to the highest bit position. (10 Marks)

OR

- 4 a. Design and realize the Boolean function using IC-74139.
 $f_1(ab) = \sum m(0, 2)$, $f_2(abc) = \sum m(1, 3, 5, 7)$. (05 Marks)
 b. Explain how look ahead carry adder circuit will reduce the propagation delay with the help of carry propagate and carry generate function. (08 Marks)
 c. Implement the Boolean function $f(abcd) = \sum m(0, 2, 4, 5, 7, 9, 10, 14)$ using multiplexers with two 4:1 MUX with variable 'a' and 'b' are connected to their select lines in first level and one 2:1 MUX with variable 'c' connected to its select line in second level. (07 Marks)

Module-3

- 5 a. With the help of logic circuit and waveforms. Explain switch bouncing applications using SR latch. (06 Marks)
 b. Write the characteristics equation for SR, JK flip flop. (06 Marks)
 c. With neat logic diagram, and waveform. Explain the operation of master-slave J-K flip-flop. (08 Marks)

OR

- 6 a. List the difference between combinational and sequential circuit. (06 Marks)
b. Explain the operation of clocked SR flip-flop using NAND-gate. (06 Marks)
c. What is the significance of Edge triggering? Explain the working of positive edge triggered D flip-flop with their function table. (08 Marks)

Module 4

- 7 a. With neat diagram, explain the operation of universal shift register. (08 Marks)
b. Design 3 bit binary synchronous down counter using JK Flip Flop. Write excitation table, transition table, and logic diagram. (12 Marks)

OR

- 8 a. What is register? With neat circuit diagram, explain the operation of 4-bit ring counter. (07 Marks)
b. With logic diagram, sequence table, decoding logic. Explain the operation of mod-7 twisted ring counter. (07 Marks)
c. Explain the working of 4 bit binary ripple counter using positive edge triggered T-flip-flop also draw timing diagram, truth table. (06 Marks)

Module 5

- 9 a. Write the difference between Moore and Mealy model with necessary block diagram. (08 Marks)
b. Design asynchronous circuit using positive edge triggered J-K flip-flop with minimal combinational gating to generate the following sequence. 0-1-2-0: if input X = 0 and 0 — 2 — 1 — 0; if input X = 1, provide an output which goes high to indicate the non-zero state in the 0-1-2-0 sequence. Is this a mealy machine? (12 Marks)

OR

- 10 a. Design a cyclic mod-8 synchronous binary counter using JK flip-flop. (10 Marks)
b. Analyze the given sequential circuit show in Fig.Q.10(b) and obtain.
i) Flip-flop Input and Output Equation
ii) Transition Equation
iii) Transition Table (N)
iv) State Table
v) State Diagram.

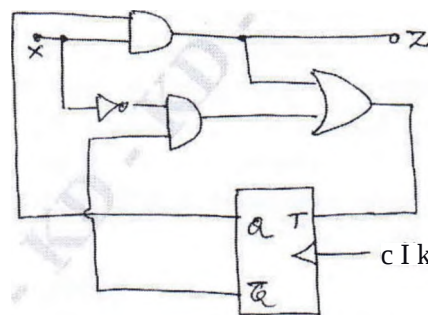


Fig.Q.10(b)

(10 Marks)

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