Code No: R22054 **R10** SET - 1

II B. Tech II Semester Regular Examinations August - 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain the instruction set architecture of 8085.
   b) What addressing mode is used by the following instructions for the relatively simple CPU?
   i) MVAC ii) CLAC iii) JMPZ Γ (8M+7M)

2. a) Explain and draw neat timing diagrams for Memory Read and Memory Write operations.
   b) Design an interface for an input device which binary address 10101010.Its computer system uses isolated I/O. (7M+8M)

3. a) Explain briefly about the shift micro operation.
   b) Write the RTL statements for the following transitions. All registers are 1-bit wide.
   i) IF α = 1 THEN copy X to W and copy Z to Y
   ii) IF α = 0 THEN copy X to W (8M+7M)

4. a) Distinguish between Hardwired control unit and Micro programmed Control unit.
   b) Draw and explain briefly about Fetch and Decode cycles for the Simple CPU. (5M+10M)

5. Design the RTL code for the shift-add multiplication UV<--X.Y for X=9 and Y=14. (15M)

6. a) Distinguish between Logical address and Physical address with an example.
   b) A computer system using the relatively simple CPU is to include a 1k associative cache with a line size of 2 bytes.
   i) How many bits are in each location of the cache?
   ii) What mask value is needed for the associative memory? (7M+8M)

7. a) Distinguish between Synchronous data transfer and Asynchronous data transfer.
   b) What is an Interrupt? Explain about different types of Interrupts. (5M+10M)

8. a) Explain the formats used by the 32-bit SPARC CPU.
   b) Explain Flynn's Classification of parallel computers. (7M+8M)
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Code No: R22054 **R10** SET - 2

II B. Tech II Semester Regular Examinations August - 2014
COMPUTER ORGANIZATION
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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about various addressing modes in Assembly Language Instructions.
   b) Write the instruction code formats for Assembly language programs and Machine code to calculate A=B+C for two-operand and zero-operand instructions (8M+7M)

2. a) Explain about the different types of Memory Chips.
   b) Construct a 16 X 2 memory subsystem constructed from two 8 X 2 ROM chips with high-order interleaving. (7M+8M)

3. Explain VHDL file to implement modulo 6 counter using high level of abstraction. (15M)

4. a) Explain the generic Micro instruction Formats.
   b) Explain Micro Sequencer for the relatively simple CPU with micro subroutines. (5M+10M)

5. a) Construct a 3 × 3 multiplexer using a Carry-Save Adder.
   b) Explain about overflow generation in unsigned two's complement Addition. (8M+7M)

6. a) Differentiate Cache memory Vs Virtual memory.
   b) Explain about External fragmentation in physical memory caused by Segmentation. (8M+7M)

7. a) Explain the concept of Handshaking technique.
   b) Explain I/O Processor with a neat diagram. (5M+10M)

8. Explain Instruction Pipelines and its conflicts with Examples. (15M)
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Code No: R22054 **R10** SET - 3

II B. Tech II Semester Regular Examinations August - 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about Data transfer instructions in Assembly Language Instructions.
   b) What addressing mode is used by the following instructions for the 8085 micro processor?
   i) SPHL ii) CMC iii) JUMP Γ (8M+7M)

2. a) Distinguish between SRAM and DRAM.
   b) Explain the CPU internal Organization. (7M+8M)

3. a) Draw the State diagram for modulo 6 counter.
   b) What is a hardware description language? Explain the features of VHDL. (10M+5M)

4. Draw and explain the Generic Hardwired Control unit. (15M)

5. a) Show the Wallace tree to perform 6 × 6 Multiplication.
   b) What is the result of the following operations on unsigned non-negative numbers using 1's complement.
   i) 1011 0100 – 0111 0111
   ii) 1000 1011 + 0111 0100
   iii) 10101.101+11011.001 (8M+7M)

6. a) Explain about Locality of Reference.
   b) Explain cache memory with Direct Mapping technique. (5M+10M)

7. a) Explain about Daisy Chaining.
   b) Explain incorporating Direct Memory Access into a computer system. (5M+10M)

8. a) Compare RISC and CISC processors.
   b) Explain Multiprocessor system inter connection N/w topologies. (7M+8M)
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Code No: R22054 **R10** SET - 4

II B. Tech II Semester Regular Examinations August - 2014
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain about Instruction Set Architecture Design.
   b) Write a program for relatively Simple CPU to add the ten values in memory locations 1001H through 100AH and store the result in memory location 1000H.Assume the result will always be less than 256. (8M+7M)

2. a) Show the internal two dimensional configuration of a 32 × 2 Memory chip.
   b) Show how the following values are stored in memory in big endian and little endian formats. Each value starts at location 22H. i) 0927H ii) 5551212H (8M+7M)

3. a) Explain the operation of Toll Booth Controller.
   b) Show the hardware to implement shl(x) micro-operation. X consists of four D flip-flops. Each micro-operation occurs when α = 1. (8M+7M)

4. a) Explain briefly about micro sequencer operations.
   b) Show the logic to generate the control signals for data register, address register and instruction register of the relatively simple CPU. (8M+7M)

5. Explain the Hardware implementation of Booth's multiplication algorithm. Discuss with an example and draw the flow chart. (15M)

6. What is paging? Explain the conversion of logical address to physical address using the page table. (15M)

7. a) Distinguish between memory mapped I/O and I/O mapped I/O.
   b) Explain the internal configuration of UART. (5M+10M)

8. a) Explain RISC processors briefly. Mention its advantages.
   b) Explain about SIMD organization with neat sketch. (8M+7M)
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