

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER- III EXAMINATION – SUMMER 2020

Subject Code: 2130306

Date: 02/11/2020

Subject Name: FUNDAMENTALS OF DIGITAL DESIGN

Time: 02:30 PM TO 05:00 PM

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

		MARKS
Q.1	(a) Differentiate Digital system and Analog system.	03
	(b) Give the difference between Combinational circuits and Sequential circuits.	04
	(c) 1) $(AB.CD)_{16} = (\text{_____})_2 = (\text{_____})_8 = (\text{_____})_{10}$ 2) Using 10's complement, perform $3250 - 9876$.	07
Q.2	(a) Define Fan-out, Switching time, Noise margin.	03
	(b) Draw symbol & truth-table for NAND, NOR, EX-OR & EX-NOR gate.	04
	(c) Design 3-basic gates using universal gates.	07
	OR	
	(c) Reduce the expression $F(W, X, Y, Z) = \sum m(0, 1, 4, 7, 11, 13, 14) + d(5, 10, 15)$ using K-map and implement minimal expression using logic gates.	07
Q.3	(a) Design Full subtractor using Half subtractor.	03
	(b) Design 2-bit magnitude comparator.	04
	(c) What is code converter? Design 4-bit BCD to XS-3 Code converter.	07
	OR	
Q.3	(a) Draw 4x1 multiplexer using basic gates.	03
	(b) Design 8 to 3 encoder using logic gates.	04
	(c) Design full adder circuit using universal gates.	07
Q.4	(a) Explain Accuracy & Resolution of DAC.	03
	(b) Explain Flash type ADC.	04
	(c) Design combinational circuit using PLA to implement 3-bit binary to gray conversion.	07
	OR	
Q.4	(a) Give the comparison between PROM, PLA & PAL.	03
	(b) Define VHDL, ABEL, FPGA & CPLD.	04
	(c) Enlist types of D to A converters and explain any one in detail with its advantages & disadvantages.	07
Q.5	(a) Explain Edge triggered RS-flipflop.	03
	(b) Draw 4-bit serial-in, serial-out shift register using D- flipflop & RS- flipflop.	04
	(c) Draw and explain master slave JK-flipflop.	07
	OR	
Q.5	(a) What is state diagram? Explain state diagram for Mealy circuit.	03
	(b) Design binary subtractor using adders.	04
	(c) Design combinational circuit using PROM to implement 3-bit binary to XS-3 conversion.	07
