Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– VI EXAMINATION – SUMMER 2020

Subject Code: 2161101 **Date:02/11/2020**

Subject Name: VLSI Technology & Design

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Compare: Semi-custom and Full custom VLSI design style.	**03**
	(b)	Write a short note on CMOS ring oscillator circuit.	**04**
	(c)	List out the fabrication steps of nMOS transistor with necessary figures.	**07**
Q.2	**(a)**	Define the following terms with example: (1) Controllability (2) Observability.	**03**
	(b)	What is substrate bias effect? Derive the expression for the threshold voltage.	**04**
	(c)	Draw and discuss: The circuit diagram of domino CMOS logic gate.	**07**
		OR	
	(c)	Draw and explain: CMOS implementation of D latch with two inverter and two CMOS TG gates.	**07**
Q.3	**(a)**	Explain latch-up problem observed in CMOS circuits. How it can be avoided?	**03**
	(b)	Explain the energy band diagram of MOS structure at surface inversion and derive the expression for the maximum possible depth of the depletion region.	**04**
	(c)	Measured voltage and current data for a MOSFET are given below. Determine the type of the device, and calculate the parameters k_n, V_{T0}, and γ. Assume $\emptyset_F$ = -0.3 V.	**07**

V_{GS}(V)	V_{DS}(V)	V_{SB}(V)	I_D(μA)
3	3	0	97
4	4	0	235
5	5	0	433
3	3	3	59
4	4	3	173
5	5	3	347

OR

Q.3	**(a)**	Draw the inverter circuit with Resistive Load. Derive critical voltage points V_{OH} and V_{OL} for Resistive Load inverter circuit.	**03**
	(b)	Explain the basic principles of pass transistor circuits. Also explain logic "0" and logic "1" transfer.	**04**
	(c)	Calculate the average junction capacitance for a simple abrupt pn-junction, which is reverse biased with a voltage V_{bias}. The doping density of the n-type region is $N_D = 10^{19}$ cm^{-3}, and the doping density of the p-type region is $N_A = 10^{16}$ cm^{-3}. The junction area is A=20μm×20μm. Assume that the reverse bias voltage changes from 0 to -5V.	**07**

Q.4	**(a)**	Briefly explain working of FPGA with suitable diagram.	**03**
	(b)	Explain voltage bootstrapping in brief.	**04**
	(c)	Consider a resistive-load inverter circuit with V_{DD}=5V, k_n'=20 µA/V^2, V_{T0}=0.8V, R_L=200kΩ, and W/L=2. Calculate the critical voltages V_{OL}, V_{OH}, V_{IL} & V_{IH} on the VTC and find the noise margins of the circuit.	**07**

OR

Q.4	**(a)**	Explain Built-in Self Test (BIST) techniques in brief.	**03**
	(b)	Write a short note on switching power dissipation of CMOS inverters.	**04**
	(c)	Consider a depletion-load inverter circuit with V_{DD}=5V, $V_{T0,driver}$ =1V, $V_{T0,load}$ = -3V, $(W/L)_{driver}$ = 2, $(W/L)_{load}$ = 1/3, $k_{n,driver}'$ = $k_{n,load}'$ = 25 µA/V^2, γ = 0.4 V$^{1/2}$ and $Ø_F$ = -0.3 V. Calculate the critical voltages V_{OL}, V_{OH}, V_{IL} & V_{IH} on the VTC and find the noise margins of the circuit.	**07**
Q.5	**(a)**	Write a short note on behavior of bistable elements.	**03**
	(b)	Realize the following Boolean function: (1) F = AB + A'C' + AB'C using CMOS Transmission Gates. (2) F = [(C+D+E)·(B+A)]' using CMOS.	**04**
	(c)	In CMOS inverter circuit, define propagation delay τ_{PLH} and obtain its expression.	**07**

OR

Q.5	**(a)**	Explain CMOS Transmission gate in brief.	**03**
	(b)	Draw voltage transfer characteristics of CMOS inverter and define V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L and NM_H.	**04**
	(c)	Draw Y- Chart for VLSI design. Also list out possible physical faults, electrical faults and logical faults in the circuit.	**07**

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