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## **GUJARAT TECHNOLOGICAL UNIVERSITY** BE - SEMESTER- III EXAMINATION – SUMMER 2020

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Subject Code: 3131704 Subject Name: DIGITAL ELECTRONICS Date:02/11/2020

Subject Name: DIGITAL ELEC	/
Time: 02:30 PM TO 05:00 PM	

## **Total Marks: 70**

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.

## MARKS

Q.1	<b>(a)</b>	Design a logic circuits for AND,OR and NOT gate using only NAND gates	03		
	(b)	What is the difference between demultiplexer and multiplexer ?	04		
		Explain with necessary diagram and truth table.			
	(c)	Explain D flip flop in detail with circuit diagram and truth table	07		
Q.2	(a)	Derive the SOP expression for following term	03		
		AB'C' + ABC' + AB'CD + A'BC' + AB			
	<b>(b)</b>	Explain binary to gray and gray to binary conversion with circuit diagram and truth table.	04		
	(c)	Minimize the following function using tabulation method: $\Sigma_{1}$	07		
	UK Design a logic circuit for half and full subtraction circuits with	07			
	(C)	K-map equations and truth table.	07		
Q.3	<b>(a)</b>	Convert the following numbers to decimal:	03		
		$(10101.101)_2$ , $(330.4)_8$ , $(A325)_{16}$			
	<b>(b)</b>	Construct 3x8 decoders with diagram and necessary truth table.	04		
	(c)	Explain following terms with example	07		
	1) Inter register-transfer operation				
2) Arithmetic micro operation					
	3) Shift micro operation				
		4) Logic micro operation			
0.0			0.2		
Q.3	(a)	Draw the circuit of 3 input ITL(Transistor Transistor Logic)	03		
	<b>(b</b> )	NAND gate and explain its operation.	04		
	$(\mathbf{D})$	Simplify the following equation using K man and	04		
	$(\mathbf{c})$	implement using logic gates:	07		
		$F(A   B   C   D) = \sum (0.1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$			
04	(a)	$\sum_{i=1}^{n} \sum_{j=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i=1}^{n} \sum_{i$	03		
2.1	( <b>u</b> ) ( <b>h</b> )	Explain 1's and 2's complement with example	04		
	(c) (c)	Explain 2-bit UP synchronous counter with K-map	07		
	(•)	equations and circuit diagram	01		
		OR			
Q.4	(a)	Write short note on PLA.	03		
-	<b>(b)</b>	Reduce the expression $A+B[AC+(B+C')D]=A+BD$	04		
	(c)	With neat sketch explain the operation of clocked RS flip flop with NAND and NOR gates.	07		



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		Gray code.			
	<b>(b)</b>	Explain 2 bit magnitude comparator with necessary diagram	04		
		and equation.			
	(c)	List out different types of memories used in digital logic	07		
circuits and define them.					
		OR			
Q.5	<b>(a)</b>	Explain meaning of following micro operations	03		
		1) $T_1$ : A+B'+1			
		2) T <sub>2</sub> : A $\wedge$ B			
		3) $T_3 : shr A$			
	<b>(b)</b>	Explain BUS transfer logic for two registers	04		
	(c)	Design a logic circuit with JK flip-flop flip flop for the given	07		
		state sequence with necessary K-map equation			

Present state	Next state
000	001
001	010
010	011
011	100
100	101
101	000

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