Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– IV EXAMINATION – SUMMER 2020

Subject Code: 3140707 **Date:27/10/2020**

Subject Name: Computer Organization & Architecture

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			Marks
Q.1	**(a)**	Enlist register reference instructions and explain any one of them in detail.	**03**
	(b)	What is combinational circuit? Explain multiplexer in detail. How many NAND gates are needed to implement 4 x 1 MUX?	**04**
	(c)	Draw the flowchart for instruction cycle and explain.	**07**
Q.2	**(a)**	What is RAM and ROM?	**03**
	(b)	One hypothetical basic computer has the following specifications: Addressing Mods = 16 Total Instruction Types = 4 (IT1, IT2, IT3, IT4) Each of the instruction type has 16 different instructions. Total General-Purpose Register = 8 Size of Memory = 8192 X 8 bits Maximum number of clock cycles required to execute one instruction = 32 Each instruction of the basic computer has one memory operand and one register operand in addition to other required fields. a. Draw the instruction word format and indicate the number of bits in each part. b. Draw the block diagram of control unit.	**04**
	(c)	Write an assembly language program to find the Fibonacci series up to the given number.	**07**
		OR	
	(c)	Write an assembly language program to find average of 15 numbers stored at consecutive location in memory.	
Q.3	**(a)**	Which are different pipeline conflicts. Describe.	**03**
	(b)	What is assembler? Draw the flowchart of second pass of the assembler.	**04**
	(c)	Write a note on arithmetic pipeline.	**07**
		OR	
Q.3	**(a)**	What is address sequencing? Explain.	**03**
	(b)	Design a simple arithmetic circuit which should implement the following operations: Assume A and B are 3 bit registers. Add : A+B, Add with Carry: A+B+1, Subtract: A+B', Subtract with Borrow: A+B'+1, Increment A: A+1, Decrement A: A-1, Transfer A: A	**04**

	(c)	Explain how addition and subtraction of signed data is performed if a computer system uses signed magnitude representation.	**07**

Q.4	**(a)**	Enlist different status bit conditions.	**03**
	(b)	What is addressing mode? Explain direct and indirect addressing mode with example.	**04**
	(c)	What is cache memory address mapping? Which are the different memory mapping techniques? Explain any one of them in detail.	**07**

OR

Q.4	**(a)**	Differentiate isolated I/O and memory mapped I/O.	**03**
	(b)	Compare and contrast RISC and CISC.	**04**
	(c)	Explain booth's multiplication algorithm with example.	**07**

Q.5	**(a)**	What is associative memory? Explain.	**03**
	(b)	Differentiate between paging and segmentation techniques used in virtual memory.	**04**
	(c)	Write a note on asynchronous data transfer.	**07**

OR

Q.5	**(a)**	Write about Time-shared common bus interconnection structure.	**03**
	(b)	Explain the working of Direct Memory Access (DMA).	**04**
	(c)	Write a note on interprocess communication and synchronization.	**07**

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