Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE- SEMESTER–VI (NEW) EXAMINATION – WINTER 2020

Subject Code:2161101 **Date:29/01/2021**

Subject Name:VLSI Technology & Design

Time:02:00 PM TO 04:00 PM **Total Marks: 56**

Instructions:

1. **Attempt any FOUR questions out of EIGHT questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Compare Semi-custom and Full custom VLSI design style	**03**
	(b)	Draw voltage transfer characteristics of inverter and define V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L and NM_H.	**04**
	(c)	Explain the VLSI design flow.	**07**
Q.2	**(a)**	Write advantages and disadvantages of dynamic logic circuit.	**03**
	(b)	Realize following Boolean logic equation using CMOS inverter. Z= (AB+C(D+E))'	**04**
	(c)	Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA).	**07**
Q.3	**(a)**	Which are the four general criteria to measure design quality of a fabricated integrated circuit (chip)?	**03**
	(b)	Draw resistive load inverter. Derive V_{IL} and V_{IH} critical voltage equation of resistive load inverter.	**04**
	(c)	Design a resistive-load inverter with R = 1 kΩ, such that V_{OL} = 0.6 V. The enhancement-type nMOS driver transistor has the following parameters VDD = 5 .0 V V_{TO}= 1. V μnCox = 22.0 μA/V^2 (a) Determine the required aspect ratio, W/L. (b) Determine V_{IL} and V_{IH}. (c) Determine noise margins NM_L and NM_H.	**07**
Q.4	**(a)**	Write advantage and disadvantage of both the enhancement load inverter configuration.	**03**
	(b)	Draw CMOS inverter with lead name of pMOS and nMOS. Derive V_{IL} critical Voltage equation of CMOS inverter.	**04**
	(c)	Consider a CMOS inverter circuit with the following parameters: V_{DD} =3.3V, V_{TON} =0.6 V, V_{TOP}= -0.7 V, kn = 200 μA/V^2, kp = 80 μA/V^2, find the NM_L.	**07**
Q.5	**(a)**	What is the need of Scaling? Mention the merits and demerits of constant voltage scaling.	**03**
	(b)	Draw tristate input circuit using Transmission Gate and CMOS inverter and also write its truth table.	**04**
	(c)	Draw circuit for CMOS two input NOR gate. Derive V_{TH} of the same.	**07**
Q.6	**(a)**	Draw CMOS implementation of D latch with two inverters and two CMOS TG gates.	**03**

	(b)	Implement following Boolean logic equation using Transmission Gate (TG). Y = AB+ A'C'+AB'C	**04**
	(c)	What is the need for voltage bootstrapping? Explain dynamic voltage bootstrapping circuit with necessary mathematical analysis.	**07**
Q.7	**(a)**	Draw general structure of scan based design.	**03**
	(b)	Give comparison between FPGA and CPLD.	**04**
	(c)	Write a short note on CMOS Transmission gate.	**07**
Q.8	**(a)**	Define and discuss Latch-up problem in CMOS inverter.	**03**
	(b)	Find a equivalent CMOS inverter circuit for simultaneous switching of all inputs, assume that (W/L)p = 15 for all pMOS transistors and (W/L)n = 10 for all nMOS transistors for the following Boolean equation F =[(C+D+E) . (B+A)]'	**04**
	(c)	Discuss the on-chip clock generation and distribution.	**07**

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