Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(Electronics Engg.) (2012 Onwards)
B.Tech.(ECE)/(Electronics & Computer Engg.)/(ETE) (2011 Onwards)
(Sem.–3)

DIGITAL CIRCUITS AND LOGIC DESIGN

Subject Code : BTEC-302
M.Code : 57584

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Q1. Answer briefly :

a) Convert $(7D2.1\ A)_{16}$ to its decimal equivalent?

b) Convert gray code 11011 into its binary equivalent?

c) Prove that $A + \overline{A}B = A + B$ by the use of Boolean algebra

d) Which gates are called used as universal gates and why?

e) Define Noise Margin.

f) Describe the operation performed by an encoder and a decoder.

g) State the important characteristics of TTL family

h) The t_{pd} for each flip flop is 30 ns determine the maximum operating frequency MOD-32 ripple counter?

i) Give the specifications of D/A converters?

j) What is a universal shift register? Explain.

SECTION-B

Q2. Simplify the expression by Quine-McClusky method

$$f = \sum m(0,2,3,6,7,8,9,10,13)$$

Q3. Explain the construction and working of Master-Slave JK-flip flop.

Q4. What is half adder? Write its truth table and develop its logic circuit. What are its limitations?

Q5. Explain the operation of Counter type of A/D converter.

Q6. Design a J-K counter that goes through states 2,4,5,7,2,4,.....

SECTION-C

Q7. a) A four bit D/A converter produces an output voltage of 4.5 volt for an input code of 1001. What will be the value of the output voltage for an input code of 0011?

b) Draw the circuit diagram of a three input TTL NAND gate and explain its operation.

Q8. a) With the help of neat diagram, explain the working of two-input ECL OR/NOR gate.

b) Explain how you will use 8 to 1 multiplexer to implement the logic function

$$F = AB + \overline{B}C + \overline{A}BC$$

Q9. Write short notes on **Any Two :**

a) Shift registers

b) Charged coupled device memory

c) ECL logic family

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.