Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 18

B.Tech.(CSE)/(IT) (2011 Onwards)

B.Tech.(3D Animation & Graphics) (2012 Onwards)

(Sem.–3)

COMPUTER ARCHITECTURE

Subject Code : BTCS-301

M.Code : 56591

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Q1 Differentiate between Computer Architecture and Organization.

Q2 What do you understand by Fetch Cycle?

Q3 Differentiate between Arithmetic Shift Left and Arithmetic Shift Right.

Q4 What is a microprogram sequencer?

Q5 What is instruction-level parallelism?

Q6 Why does increasing the capacity of cache tend to increase its hit rate?

Q7 What do you mean by memory hierarchy?

Q8 Draw a neat diagram for handshaking mode of data transfer.

Q9 How many 128×8 ROM memory chips are needed to provide a memory capacity of 4096×16?

Q10 What do you mean by Inter-processor Communication?

SECTION -B

Q11 Give the comparison between hardwired control unit and micro programmed control unit.

Q12 Compare RISC and CISC architecture.

Q13 Explain all the phases of instruction cycle.

Q14 What are the various types of interrupts? Explain.

Q15 Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each pipeline.

SECTION -C

Q16 Explain with an example, how effective address is calculated in different types of addressing modes?

Q17 Explain in detail the different mappings used for cache memory. Compare them.

Q18 With neat block diagram, explain how DMA controller is initialized for DMA data transfer?

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.