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Total No. of Questions : 09

B.Tech. (Electronics Engg.) (2012 Onwards)

B.Tech. (ECE/ETE) (2011 Onwards) (Sem.–5)

DIGITAL SIGNAL PROCESSING

Subject Code : BTEC-502

M.Code : 70546

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt ANY FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt ANY TWO questions.**

SECTION-A

1. Write briefly :

a) Whether the signal $y(n) = \sin 3n$ is periodic or non-periodic?

b) Is the system $y(n) = x(n) \cos(\omega n)$ linear or non-linear?

c) Give two advantages of digital signal processing over analog signal processing.

d) Why the ROC of Z-transform cannot contain any pole ?

e) Why it is not possible to take the DFT of sequency having infinite length?

f) In the implementation of a digital system what are the effects of finite-word-length?

g) Give the various steps involved in the design of IIR filter.

h) Differentiate between FIR and IIR filter.

i) What is Gibbs Phenomenon?

j) List the various features of DSP processors.

SECTION-B

2. Compute the convolution of $x(n) = u(n) - u(n-5)$, $h(n) = [1, 2, 2, 1]$

3. Determine the Z-transform and sketch the ROC of :

$$x(n) = -\alpha^n u(-n-1)$$

4. Obtain inverse Z-transform using partial fraction expansion method where :

$$X(z) = \frac{3}{z - \frac{1}{4} - \frac{1}{8}z^{-1}}; x(n) \text{ is causal}$$

5. The transfer function of analog filter is :

$$H_a(s) = \frac{3}{(s+2)(s+3)}$$

With T = 0.1sec. Design the digital filter using Bilnear Transformation Technique.

6. Obtain the direct form 1direct form 1I, cascade & parallel structure for the following system :

$$y(n) = -0.1y(n-1) + 0.2y(n-1) + 3x(n) + 3.6x(n-1) + 0.6x(n-2)$$

SECTION-C

7. Explain the different types of structures for the realization of FIR filter.

8. Compute the 8-point DFT of a sequence

$$x(n) = \left\{\frac{1}{2}, \frac{1}{2}, \frac{1}{2}, \frac{1}{2}, 0, 0, 0, 0,\right\}$$

Using in-place radix-2 decimation-in-time (DIT) FFT algorithm.

9. With the help of neat diagram describe the memory architecture of TMS320C54X and give the comparison between DSP processor and general purpose microprocessor.

NOTE : Disclosure of identity by writing mobile number or making passing request on any page of Answer sheet will lead to UMC case against the Student.