Roll No. | | | | | | | | | | | | |

Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(EE/Electrical & Electronics) (2011 Onwards E-I)
(Sem.–6)

MICROELECTRONICS TECHNOLOGY

Subject Code : BTEE-605F
M.Code : 71157

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Answer briefly :

a. What is the difference between etching and deposition?

b. Write chemical reaction for growth of sio2.

c. Draw the apparatus for CVD in formation of silicon.

d. What do you mean by gattering?

e. What do you mean patterning?

f. Why we use GaAs for formation of IC?

g. What do you mean by hybrid circuits?

h. What is the use of ficks two dimensional law?

i. Write design rules for NMOS technology.

j. Write the various apparatus names in reactive ion etching.

SECTION-B

2. Discuss in detail about Fabrication of diodes, transistors, resistors and capacitors.

3. Write the various peroxidation cleaning procedures.

4. What are the various electrical properties of MOSFET?

5. What do you mean by deposition?

6. Draw layout for NAND and NOR gate.

SECTION-C

7. How can you design PLA?

8. Discuss atomic diffusion mechanism.

9. What are the fabrication steps for CMOS?

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.