Roll No. | | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 09

B.Tech.(ECE)/(ETE) (2011 Onwards) (Sem.–6)

VLSI DESIGN

Subject Code : BTEC-604

M.Code : 71124

Time : 3 Hrs. Max. Marks : 60

INSTRUCTION TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Answer briefly :

a) With one example each differentiate between STD_LOGIC and STD_ULOGIC.

b) Perform the following using *sra* and *sll* shift operators :

(i) 10100101

(ii) 01011010

c) Explain subtype for any data type with an example.

d) Define pull-up and pull-down ratios of NMOS.

e) Explain scalar data type in VHDL with an example.

f) Describe the significance of process statement.

g) What is propagation delay?

h) Differentiate between Arrays and Records in VHDL.

i) Discuss the wiring capacitances,

j) What is meant by body effect?

SECTION-B

2. Explain various data objects in VHDL language each with two examples.

3. What is the significance of process statement in VHDL? Explain with an example.

4. Write a VHDL code for full adder using behavioural modelling style.

5. Does the inverter with a lower VOL always have the shorter high-to-low switching time? Justify your answer.

6. Describe in detail twin tub CMOS process of fabrication.

SECTION-C

7. Design 8×1 MUX using two 4:1 MUX and one 2:1 MUX along with its diagram. Implement 8×1 multiplexer in VHDL using structural modelling style.

8. Consider a CMOS inverter circuit with the following parameters :

   $V_{DD} = 3.3V$, $V_{TO,n} = = 0.6V$, $V_{TO,P} = -0.7V$, $k_n = 200\mu A/V^2$, $k_p = 80\mu A/V^2$ Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has $k_R = 2.5$ and $V_{TO,n} \neq |V_{TO,P}|$ hence it is not a symmetric inverter.

9. Discuss about the effects of scaling down the dimensions of MOS circuits and systems.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.