B.C.A. (Part–I) Semester–I Examination
DIGITAL TECHNIQUES–I
Paper–1ST3

Time : Three Hours]   [Maximum Marks : 60

Note :— (1) All questions carry equal marks.

(2) Draw neat diagram wherever necessary.

1. (a) Convert the following numbers and find 'X' :

$(29.75)_{10} = (X)_2 = (X)_8 = (X)_{16}$ 6

(b) Explain OR, AND, NOT gates with logic symbol and truth table.   6

OR

2. (a) Explain binary subtraction using 1's and 2's complement method with suitable example.   6

(b) Explain the operation of X-OR and X-NOR gate with logic symbol and truth table.   6

3. (a) Explain the following characteristics of logic gates :

(i) Fan –In

(ii) Propagation Delay

(iii) Noise immunity.   6

(b) Explain the operation of CMOS NAND gate.   6

OR

4. (a) Give the classification of logic families.   6

(b) Explain ECL logic gate.   6

5. (a) State and prove the DeMorgan's theorem.   6

(b) Simplify the logic equation by K-map and implement it by NOR gate.

$f(A, B, C, D) = \pi M(4, 6, 10, 12, 13, 15)$ 6

OR

6. (a) Verify the following identities :

(i) $(A + B)(\bar{A} + C) = AC + \bar{A}B$

(ii) $(A + B)(A + \bar{B}) = A$ 6

(b) Simplify the following logic equation by K-map and implement it by NAND gate :

$f(A, B, C, D) = \Sigma m (0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$ 6

---

7. (a) Explain construction and operation of full adder circuit with logic circuit and truth table. 6

    (b) Explain the block diagram and functions of 1 bit ALU IC 74181. 6

OR

8. (a) Explain construction and operation of 4-bit binary parallel adder. 6

    (b) Explain binary subtraction using 1's and 2's complement method. 6

9. (a) What is decoder ? Explain 2:4 decoder with logic diagram. 6

    (b) What is multiplexer ? Explain 4:1 MUX with diagram and operation table. 6

OR

10. (a) Explain extention of 4:16 decoder into 1:16 demultiplexer. 6

    (b) Explain the operation of 16:1 MUX with logic diagram. 6