Code: 13A04804 **R13**

B.Tech IV Year II Semester (R13) Regular & Supplementary Examinations April 2018

RF INTEGRATED CIRCUITS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) State the maximum power transfer theorem and its conditions.
(b) What are the conditions for resonance in series RLC networks?
(c) Define gain and bandwidth.
(d) What is reflection coefficient?
(e) What is thermal noise?
(f) Define phase locked loop.
(g) What is power match and noise match.
(h) Define phase detector.
(i) What is meant by integer-N synthesis?
(j) Define frequency synthesis.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Design and convert series to parallel RL & RC network transformations.
(b) Explain about passive IC components interconnects in RF system.

OR

3 (a) Compare Pi match and T-match of a network system.
(b) Discuss about the basic architecture of a RF system.

UNIT – II

4 Prove that a long channel MOS device transconductance depends only on the square root of bias current.

OR

5 (a) Draw and explain about the tuned amplifier.
(b) Explain about the high frequency amplifier design.

UNIT – III

6 (a) Explain about intrinsic MOS noise parameters.
(b) Explain about power match versus noise match.

OR

7 Design any two examples of multiplier based mixers.

UNIT – IV

8 (a) Discuss about class D, E, F amplifier in detail.
(b) Explain about phase locked loops and phase detectors.

OR

9 Write short notes on:
(a) Negative resistance oscillators.
(b) Linearlized PLL models.

UNIT – V

10 (a) Explain about frequency synthesis in detail.
(b) Discuss about phase noise and fractional frequency in frequency synthesis.

OR

11 Write short notes on:
(a) GSM radio architecture.
(b) CDMA radio architecture.

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