Code: 9A04605

AS

B.Tech IV Year II Semester (R09) Supplementary Examinations April 2018

VLSI DESIGN

(Electronics & Communication Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions
All questions carry equal marks
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1 Explain the following terms:
(a) Thermal oxidation technique.
(b) Kinetics of thermal oxidation.

2 (a) Derive an equation for R_{ds} of an n-channel enhancement MOSFET in linear region.
(b) Explain the term figure of merit of a MOS transistor.

3 Clearly explain the VLSI design flow with a neat flow chart.

4 (a) Explain the requirement & operation of pass transistor and transmission gates.
(b) Write about CMOS logic, domino logic and n-pCMOS logic.

5 (a) Design logic for an ALU that can perform both logical and arithmetic operations.
(b) Enumerate all the 16 possible functions of a two input ALU.

6 (a) Design a 3 × 8 binary decoder using NOR-NOR implementation of PLA.
(b) Implement the following function using PLA and EPROM:
$F_1 = \overline{ABC} + BC + AC$

7 (a) Explain about event driven simulation.
(b) Using VHDL as a tool, write a program to synthesize a mod 10 counter.

8 (a) What are BIST techniques?
(b) Explain how BILBO is used for scan–path–test and also as a test vector generator.

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