

Code: 9A04605

B.Tech IV Year II Semester (R09) Supplementary Examinations July 2018

**VLSI DESIGN**

(Electronics &amp; Communication Engineering)

(For 2009 (LC), 2010, 2011, 2012 regular &amp; 2011 (LC), 2012, 2013 lateral admitted batches only)

Time: 3 hours

Max. Marks: 70

Answer any FIVE questions  
All questions carry equal marks

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- 1 With neat sketches explain BiCMOS fabrication process in an n well.
- 2 (a) What is a pass transistor logic?  
(b) Draw the circuit of pass transistor AND gate and explain its operation.
- 3 Design a stick diagram for two input PMOS NAND and NOR gates.
- 4 Realize the logic gates inverter, NAND and NOR gates using NMOS as well as with PMOS technology.
- 5 (a) Provide the design of an 8×8 array multiplier.  
(b) Explain the working principle of Booth Multiplier.
- 6 Differentiate between full custom design and semicustom design? Specify the respective applications when they are preferred.
- 7 Write a program in VHDL for an 8:1 multiplexer in behavioral and structural style and compare them.
- 8 (a) Explain the testing of ICs with Scan path approaches.  
(b) Write about Level sensitive scan design.

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