Code: 15A04802 **R15**

B.Tech IV Year II Semester (R15) Regular Examinations April 2019

LOW POWER VLSI CIRCUITS & SYSTEMS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Define sub-threshold swing.
(b) Define channel length modulation.
(c) What is meant my fringing field capacitance?
(d) What are the disadvantages of resistive load inverter?
(e) What are the drawbacks of parallelism approach?
(f) What is the effect of feature scaling on power dissipation?
(g) List out the methods to minimize switched capacitance.
(h) What is meant by molecule in Transmeta Crusoe processor?
(i) Draw the AND gate using adiabatic logic.
(j) How multiple threshold voltages can be achieved in a circuit?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) Explain the principles and challenges in low power design.
(b) List different sources of dynamic and static power dissipation.

OR

3 Explain the structure and operation of NMOS transistor and derive expression for drain current.

UNIT – II

4 Explain the operation of depletion load nMOS inverter and draw the VTC.

OR

5 (a) Discuss in detail about the CMOS transmission gates.
(b) Discuss delay parameters of MOS transistors.

UNIT – III

6 (a) Derive an expression for short circuit power dissipation of a CMOS inverter.
(b) Explain in detail about switching power dissipation.

OR

7 Explain the optimization procedures for low power dissipation at algorithm and architecture level.

UNIT – IV

8 Explain any three techniques that are used to reduce power at the logic level.

OR

9 Using Shannon's expansion principle, explain the pre-computation of adder-comparator circuit.

UNIT – V

10 (a) Explain variable threshold CMOS inverter circuit with a neat sketch.
(b) What are the advantages and disadvantages of MTCMOS circuits?

OR

11 Explain the techniques used to minimize the software contribution to power dissipation.

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