

B.Tech IV Year II Semester (R15) Regular Examinations April 2019

LOW POWER VLSI CIRCUITS & SYSTEMS

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

- 1 Answer the following: (10 X 02 = 20 Marks)
- Define sub-threshold swing.
 - Define channel length modulation.
 - What is meant by fringing field capacitance?
 - What are the disadvantages of resistive load inverter?
 - What are the drawbacks of parallelism approach?
 - What is the effect of feature scaling on power dissipation?
 - List out the methods to minimize switched capacitance.
 - What is meant by molecule in Transmeta Crusoe processor?
 - Draw the AND gate using adiabatic logic.
 - How multiple threshold voltages can be achieved in a circuit?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

- Explain the principles and challenges in low power design.
 - List different sources of dynamic and static power dissipation.

OR

- Explain the structure and operation of NMOS transistor and derive expression for drain current.

UNIT – II

- Explain the operation of depletion load nMOS inverter and draw the VTC.

OR

- Discuss in detail about the CMOS transmission gates.
 - Discuss delay parameters of MOS transistors.

UNIT – III

- Derive an expression for short circuit power dissipation of a CMOS inverter.
 - Explain in detail about switching power dissipation.

OR

- Explain the optimization procedures for low power dissipation at algorithm and architecture level.

UNIT – IV

- Explain any three techniques that are used to reduce power at the logic level.

OR

- Using Shannon's expansion principle, explain the pre-computation of adder-comparator circuit.

UNIT – V

- Explain variable threshold CMOS inverter circuit with a neat sketch.
 - What are the advantages and disadvantages of MTCMOS circuits?

OR

- Explain the techniques used to minimize the software contribution to power dissipation.
