Code: 15A04802 **R15**

B.Tech IV Year II Semester (R15) Advanced Supplementary Examinations July 2019

LOW POWER VLSI CIRCUITS & SYSTEMS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) List out the limits of low power design.
(b) Write the expression for body effect coefficient.
(c) Define noise margin of an inverter.
(d) What are the advantages of dynamic logic circuits?
(e) What is meant by drain induced barrier lowering?
(f) Explain pipelining approach.
(g) What is the basic assumption of state assignment algorithm?
(h) What are the techniques used to reduce power at the logic level?
(i) List out the approaches for minimizing leakage power.
(j) What are the advantages of dual-threshold voltage assignment approach?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 What is the need for low power VLSI chips? Explain the various sources of dynamic and static power dissipation.

OR

3 Explain the following in detail:

(a) Sub threshold swing.
(b) Effects of short channel length.

UNIT – II

4 Explain the operation of CMOS inverter with neat sketches.

OR

5 (a) Explain about Elmore delay.
(b) Design EX-OR gate using pass transistor logic.

UNIT – III

6 (a) Explain in detail about Monte Carlo method for estimating glitch power.
(b) What are the factors influencing the leakage current in deep sub-micrometer transistor?

OR

7 (a) List out the advantages of voltage scaling.
(b) Explain the charge sharing phenomena in dynamic circuits.

UNIT – IV

8 Explain the power optimization using operation reduction techniques.

OR

9 Explain FSM and combinational logic synthesis with suitable state machine representation.

UNIT – V

10 (a) Design a full adder using *Adiabatic logic*.
(b) Compare and contrast MTCMOS and DTCMOS circuits.

OR

11 Explain the techniques used to minimize the software contribution to power dissipation.

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