



B.Tech IV Year II Semester (R15) Advanced Supplementary Examinations July 2019

LOW POWER VLSI CIRCUITS & SYSTEMS

(Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 70

PART – A

(Compulsory Question)

1 Answer the following: (10 X 02 = 20 Marks)

- List out the limits of low power design.
- Write the expression for body effect coefficient.
- Define noise margin of an inverter.
- What are the advantages of dynamic logic circuits?
- What is meant by drain induced barrier lowering?
- Explain pipelining approach.
- What is the basic assumption of state assignment algorithm?
- What are the techniques used to reduce power at the logic level?
- List out the approaches for minimizing leakage power.
- What are the advantages of dual-threshold voltage assignment approach?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 What is the need for low power VLSI chips? Explain the various sources of dynamic and static power dissipation.

OR

3 Explain the following in detail:

- Sub threshold swing.
- Effects of short channel length.

UNIT – II

4 Explain the operation of CMOS inverter with neat sketches.

OR

- Explain about Elmore delay.
- Design EX-OR gate using pass transistor logic.

UNIT – III

- Explain in detail about Monte Carlo method for estimating glitch power.
- What are the factors influencing the leakage current in deep sub-micrometer transistor?

OR

- List out the advantages of voltage scaling.
- Explain the charge sharing phenomena in dynamic circuits.

UNIT – IV

8 Explain the power optimization using operation reduction techniques.

OR

9 Explain FSM and combinational logic synthesis with suitable state machine representation.

UNIT – V

- Design a full adder using *Adiabatic logic*.
- Compare and contrast MTCMOS and DTCMOS circuits.

OR

11 Explain the techniques used to minimize the software contribution to power dissipation.

