FirstRanker.com

www.FirstRanker.com

www.FirstRanker.com

Roll No.	Total No. of Pages : 02
Total No. of Questions : 18	
B.Tech. (ECE) (E-I 20 (Automation & Robotics) (DE-I 20 DIGITAL SYSTEI Subject Code:E M.Code:71	12 & Onward) (Sem.–6) VI DESIGN 3TEC-904
Time:3 Hrs.	Max. Marks:60
INSTRUCTIONS TO CANDIDATES : 1. SECTION-A is COMPULSORY consisting of each.	of TEN questions carrying TWO marks
2. SECTION-B contains FIVE questions car have to attempt any FOUR questions.	rying FIVE marks each and students

SECTION-C contains THREE questions carrying TEN marks each and students 3. have to attempt any TWO questions.

SECTION-A

Answer briefly :

- Differentiate between combinational and sequential circuits. 1.
- 2. Why the input variables to a PAL are buffered?
- Design 4:1 MUX using 2:1 MUXs. 3.
- 4. What is race around condition in JK flip flop?
- With the help of an example differentiate between truth table and excitation table. 5.
- 6. What is programmable logic array? How it differs from ROM?
- 7. Differentiate between Mealy and Moore machines.
- 8. Define Flow Table in Asynchronous Sequential Circuit.
- 9. What is field programmable logic array?
- 10. What is the cause for essential hazards?



www.FirstRanker.com

www.FirstRanker.com

SECTION-B

- 11. Design and explain a Full Adder using Half Adders and truth table.
- 12. Explain the working of Master Slave JK flip flop using circuit diagram.
- 13. Implement the following function using PAL and PLA :

 $X (A, B, C, D) = \sum m (7, 8, 9, 10, 11, 12, 13, 14, 15)$

- 14. Explain static and dynamic hazards with examples.
- 15. What are FPGAs? Discuss the internal architecture of FPGA, highlighting the functionality of each module.

SECTION-C

- 16. Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6 by using JK Flip-flop.
- 17. Design an Asynchronous sequential circuit using SR latch with two inputs A and B and one output Y. B is the control input which, when equal to 1, transfers the input A to output y. when B is 0, the output does not change, for any change in input.
- 18. Draw an ASM chart to design control logic of a binary multiplier. Realize the same using MUX, decoder and D-type flip flops.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.

2 | M - 7 1 2 3 3