

Roll No.

--	--	--	--	--	--	--	--	--	--	--	--

Total No. of Pages : 02

Total No. of Questions : 09

**B.Tech. (ECE)/(Electronics Engg)/
(Electronics & Computer Engg) (2012 to 2017) (Sem.-3)**

DIGITAL CIRCUITS AND LOGIC DESIGN

Subject Code : BTEC-302

M.Code : 57584

Time : 3 Hrs.

Max. Marks : 60

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A** is **COMPULSORY** consisting of **TEN** questions carrying **TWO** marks each.
2. **SECTION-B** contains **FIVE** questions carrying **FIVE** marks each and students have to attempt any **FOUR** questions.
3. **SECTION-C** contains **THREE** questions carrying **TEN** marks each and students have to attempt any **TWO** questions.

SECTION-A

1. Answer briefly :

- a) Perform the subtraction $10111_2 - 11111_2$ using 1's complement method of subtraction.
- b) Convert the decimal number 359_{10} to BCD.
- c) Give the difference between SOP and POS forms.
- d) Draw symbol and construct the truth table for three input Ex-OR gate.
- e) Why totem pole outputs cannot be connected together.
- f) How multiplexer differs from decoder?
- g) What is the basic difference between buffered and un buffered CMOS devices?
- h) What is totem-pole output stage? What are its advantages?
- i) Which is the fastest ADC and why?
- j) How many address bits are required for a 512×4 memory?

SECTION-B

2. Using the Boolean algebra, simplify the expression :

$$\overline{A}\overline{B}C + \overline{(A+B+\overline{C})} + \overline{A}\overline{B}\overline{C}D$$

3. What is meant by Decoder? Explain 3-to-8 line decoder with diagram and truth table.
4. Design a counter with the following binary sequence: 0, 4, 2, 1, 6 and repeat. Use JK flip-flops.
5. Explain the working of a basic totem-pole TTL 2 input NAND gate.
6. Realize $F(w, x, y, z) = \Sigma(1, 4, 6, 7, 8, 9, 10, 11, 15)$ using 8 to 1 Mux

SECTION-C

7. Find a minimal SOP representation for $f(A, B, C, D, E) = \sum m(1, 4, 6, 10, 20, 22, 24, 26) + d(0, 11, 16, 27)$ using K-map method. Draw the circuit of the minimal expression using only NAND gates.
8. a) Implement the following function using PLA $F1 = \Sigma(0, 1, 2, 4)$ and $F2 = \Sigma(0, 5, 6, 7)$.
- b) Describe with the help of a schematic diagram the principle of operation of a successive type A/D converter.
9. Write short notes on **any two** :
- a) Weighted register D/A converter
- b) Edge triggered JK flip-flop
- c) CMOS logic family

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.