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Roll No. | | | | | | | | | | | | Total No. of Pages : 02

Total No. of Questions : 08

M.Tech.(ECE) (Sem.–1)

ELECTRONICS SYSTEM DESIGN

Subject Code : EC-502

M.Code : 36203

Time : 3 Hrs. Max. Marks : 100

INSTRUCTION TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT questions.
2. Each question carries TWENTY marks.

1. a) Implement the function $f = \Sigma m(0, 2, 3, 6, 7, 11) + \phi(1, 4, 8, 15)$ by using Q-M method. 10

   b) Using the theorems minimize the following expression 10

$$F = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}BC\bar{D} + \bar{A}BCD + \bar{A}B\bar{C}D + A\bar{B}\bar{C}D + AB\bar{C}D + ABC\bar{D}$$

2. a) Design and implement half and full subtractor using NOR gates. 12

   b) Explain ROM and PLA. What is the difference between ROM and PLA? 8

3. a) Why shift registers are required? Discuss the various operation modes of shift registers. 10

   b) List the design steps for next state decoders. 10

4. Design a circuit that will compare two 2-bit number. Implement the circuit using only NOR gates and then again repeat using only NAND gates? 20

5. a) What is a binary cell? Design a binary cell mentioning all appropriate design steps. 10

   b) Define propagation delay? What is its significance? Also make a comparison between open collector and tri-state bus systems. 10

6. Implement the function $f = \Sigma m$ (0, 4, 6, 7, 9, 12, 14) using ROM, PLA and 4 : 1 multiplexer. 20

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7. a) Explain the purpose of grounding and shielding in digital systems. 8

b) What is tri-state logic circuit and how does it help building a tri-state bus system? Discuss the advantages of this logic in reducing hardware in system implementation. 12

8. Write short note on following : 20

a) PAL

b) Hazards

c) Wired Logic

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NOTE : Disclosure of identity by writing mobile number or making passing request on any page of Answer sheet will lead to UMC case against the Student.

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