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M.Tech.(ECE) E-I   (Sem.–2)
VLSI DESIGN
Subject Code : EC-511
M.Code : 36212

Time : 3 Hrs.   Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :
1. Attempt any FIVE questions in all, out of EIGHT questions.
2. Each question carries TWENTY marks.

1. a) Compare combination and sequential circuits with the help of examples. Also discuss the timing analysis of sequential circuits.

   b) Explain Charge coupled devices with suitable diagrams.

2. a) Reduce the following state table to a minimum number of states.

Present State	Next State X=0	1	Present Output X=0	1
a	h	c	1	0
b	c	d	0	1
c	h	b	0	0
d	f	h	0	0
e	c	f	0	1
f	f	g	0	0
g	g	c	1	0
h	a	c	1	0

   b) Realize the following state table using a minimum number of AND and OR gates together with a D flip-flop.

$X_1X_2X_3$

	000	001	010	011	100	101	110	111	Z
A	A	A	B	B	B	B	A	A	0
B	A	B	B	A	A	B	B	A	1

3. a) Tabulate the PAL programmable table and mark the fuse map in a PAL diagram for the BCD to Excess-3 code converter.

    b) Discuss the structures of standard PLDs and complex PLDs in detail with suitable diagram.

4. Explain the basic Xilinx structure, configurable logic block and input/output block (IOB) of XC4000 family with the help of suitable diagrams.

5. a) Explain the pre-defined and user-defined data types of VHDL language.

    b) Explain pre-defined and user-defined attributes with the help of suitable examples.

6. a) What is the need of hardware description language? Explain the design flow and basic terminology of VHDL language with suitable diagrams.

    b) Write behavioural VHDL description for the 3-bit magnitude comparator.

7. a) Explain various loop statements in Verilog.

    b) Write the Verilog description of 4-bit ripple carry adder.

8. Write short notes on the following (any **TWO**) :

    a) SRAM

    b) Operators in VHDL

    c) Tasks and functions in Verilog

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.