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Total No. of Pages : 01

Total No. of Questions : 08

**M.Tech (CSE Engg.) Big Data (Campus) (Sem.-2)****ADVANCED COMPUTER ARCHITECTURE****Subject Code : CSB-205****M.Code : 51089****Time : 3 Hrs.****Max. Marks : 50****INSTRUCTIONS TO CANDIDATES :****1. Attempt any FIVE questions out of EIGHT questions.****2. Each question carries TEN marks.**

1.
  - a) Explain the description of control sequence for simple RISC computer.
  - b) Write a short note on hardwired control unit design.
2.
  - a) What is cache coherence problem? Discuss its protocols.
  - b) List the levels of cache in computer architecture? Discuss performance issues in memory.
3.
  - a) Differentiate between homogeneous and heterogeneous cores in architecture.
  - b) Discuss the optimal resource sharing strategies in multi core architecture.
4. Why it is required for a computer to do parallel computing? Write the reasons for its failure?
5. Define :
  - a) Concurrency and Parallelism
  - b) Load Balancing
6.
  - a) What are the design challenges in Multithreading concepts?
  - b) How Intel Corporation is supporting multithreading capabilities using Intel compilers?
7. Explain the various factors on which performance of processors is measured.
8.
  - a) How OpenMP is used for parallelism within a multi-core programming?
  - b) Give an overview of Extensive API Library for finer control.

**NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.**

