Roll No. | | | | | | | | | | | | |

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M.Tech.(IT) (2015 & Onwards)/(CSE Engg.)/(E-Security) (Sem.–1)

ADVANCED COMPUTER ARCHITECTURE

Subject Code : CS-505

M.Code : 35406

Time : 3 Hrs. Max. Marks : 100

INSTRUCTIONS TO CANDIDATES :

1. Attempt any FIVE questions out of EIGHT questions.
2. Each question carries TWENTY marks.

1. A computer uses a memory of 65,536 words with eight bits in each word. It has the following registers: PC, AR, TR (16 bits each), and AC, DR and IR (eight bits each). A memory reference instruction consists of three words: an eight bit operation code (one word), and a 16-bit address (in the next two words). All the operands are of eight bits. There is no indirect bit.

   (a) Draw a block diagram of a computer showing the memory and registers.

   (b) Draw the diagram showing the placement in memory of a typical three-word instruction and corresponding 8-bit operand.

   (c) List the sequence of the micro-operations for fetching a memory reference instruction and then placing the operand in DR. Start from the timing signal T_0.

2. (a) What is the difference between programmed I/O,. interrupt driven I/O and DMA?

   (b) Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. The operation code has 6 bits and the control memory has 2048 words.

3. (a) Differentiate between computer architecture and computer organization.

   (b) Which types of signals are necessary to activate the external interrupts of 8085?

   (c) What is the advantage of relative addressing mode?

   (d) Why DMA controller has a bidirectional address bus?

4. Out of shared and distributed Memory MIMD architecture which is best and under which scenarios explain with an example.

5. (a) Determine the number of clock cycles that it takes to process 200 task in a six segment pipeline. Explain with help of diagram.

   (b) Explain what vector architecture is and why it is used?

6. (a) Why does DMA have priority over CPU when both request a memory transfer?

   (b) Formulate a hardware procedure for detecting an overflow by computing the sign of the sum with the signs of the augends and addend. The numbers are in signed 2's complement representation.

7. What is ILP processors and where they are used? What is code scheduling for ILP processors? Explain with help of diagram.

8. Write a short note on : Pipelined processors, VLIW architecture and super scalar processors.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.