



Code No: 841AB

R17**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD****MCA I Semester Examinations, April/May - 2019****COMPUTER ORGANIZATION****Time: 3hrs****Max.Marks:75****Note:** This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A**5 × 5 marks = 25**

- 1.a) Discuss the Combinational and Sequential Circuits. [5]
- b) What is hit ratio? [5]
- c) With the help of neat diagram, explain the 8086 CPU architecture. [5]
- d) What is the importance of I/O interface? In a computer system, why a PCI bus is used? [5]
- e) Consider the multiplication of two 40*40 matrices using a vector processor. How many product terms are there in each inner product and how many inner products must be evaluated? [5]

PART - B**5 × 10 marks = 50**

- 2.a) Simplify the following Boolean function using four variables K-Map.
 $F(A, B, C, D) = \sum(0, 1, 2, 4, 5, 7, 11, 15)$
- b) Convert the following binary numbers to decimal: 101110; 1110101; and 110110100. [5+5]

OR

- 3.a) Write the operation of 3-to-8 line decoder.
 - b) Explain how the floating-point numbers are represented and used in digital arithmetic operations. Give an example. [5+5]
4. Explain the direct mapping of Cache memory? [10]

OR

- 5.a) Give a neat sketch that illustrates the components in a typical memory hierarchy.
- b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? [5+5]

6. A two word instruction is stored in memory at an address designated by symbol W . The address field of the instruction (stored at $W + 1$) is designated by the symbol Y . The operand used during the execution of the instruction is stored at an address symbolized by Z . An index register contains the value X . State how Z is calculated from the other addresses if the addressing mode of the instruction is

(a) Direct (b) Indirect (c) Relative (d) Indexed [10]

OR

- 7.a) Discuss the generation of physical address.
- b) What is meant by Addressing modes? Explain in detail. [5+5]

8. Compare interrupt driven data transfer scheme with DMA. Using block diagram explain interrupt driven transfer scheme. [10]

OR

9. Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs? [10]

- 10.a) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved?

- b) What is a vector? Differentiate between a conventional scalar processor and a vector processor? [5+5]

OR

11. List the reasons of pipeline conflicts in pipelined processor. Discuss the various conflicts that might arise in a pipeline. How are they resolved? [10]

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