

**R17****Code No: 841AB****JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD****MCA I Semester Examinations, October/ November - 2020****COMPUTER ORGANIZATION****Time: 2 Hours****Max.Marks:75**

**Answer any five questions**  
**All questions carry equal marks**

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1. Simplify the following Boolean function in product-of-sums form by means of a four-variable map. Draw the logic diagram with (a) OR-AND gates (b) NOR gates  
$$F(w, x, y, z) = \Sigma (2, 3, 4, 5, 6, 7, 11, 14, 15)$$
 [7+8]
2. With help of a detailed example, illustrate the effects of different cache mapping techniques. [15]
3. Describe the architecture of 8086 and explain the need of code segment and extra segment. [15]
4. What is the difference between isolated I/O and memory mapped I/O? What are the advantages and disadvantages of each? [15]
5. Compare centralized and distributed inter processor arbitration logic for multi processor systems. [15]
6. Construct a 5-to-32-line decoder with four 3-to-8 line decoders with enable and one 2-to-4-line decoder. Explain your circuit functionality. [15]
- 7.a) How many  $128 \times 8$  RAM chips are needed to provide a memory capacity of 2048 bytes.  
b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? [7+8]
8. Write an assembly language program using subroutine to display factorial of a given number. Trace your program for input '4'. [15]

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