Code No: 821AB **R15**

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MCA I Semester Examinations, August - 2017
COMPUTER ORGANIZATION

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) What are the steps in the design of a combinational circuit? [5]
b) What do you mean by a content addressable memory? [5]
c) Distinguish between near and far jumps in 8086 architecture. [5]
d) What do you mean by vectored interrupt? [5]
e) What are the three major difficulties that cause the pipeline to deviate from its normal operation? [5]

PART - B

5 × 10 Marks = 50

2.a) Give the excitation table for four flip-flops.
b) Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable and one 2-to-4 line decoder. [5+5]

OR

3.a) Simplify the following Boolean function using four-variable maps.
i) $F(A,B,C,D) = \sum (3,7,11,13,14,15)$
ii) $F(A,B,C,D) = \sum (0,1,2,4,5,7,11,15)$
b) Define $(r-1)$'s complement and r's complement. [5+5]

4.a) A computer uses RAM chips of size 1024×4 capacity. How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.
b) Obtain the Boolean function for the match logic of one word in an associative memory taking into consideration a tag bit that indicates whether the word is active or inactive. [5+5]

OR

5.a) Explain how memory protection can be ensured by memory management hardware.
b) Consider a 32-bit microprocessor that has an on-chip 16 Kbyte four-way set-associative cache. Assume that the cache has a line size of four 32-bit words. Draw a block diagram of this cache showing its organization and how the different address fields are used to determine a cache hit/miss. Where in the cache is the word from memory location ABCDE8F8 mapped? [5+5]

6.a) Give an overview of 8086 registers.
b) Develop an assembly language program that reads three integer values and determines the largest among the input. [5+5]

OR

7.a) Give an overview of memory segmentation in 8086 architecture.
b) Develop an assembly language program to check whether a number is an even or an odd number. [5+5]

8.a) Demonstrate with an example interrupt-driven I/O.
b) Explain how block transfers are accomplished by DMA. [5+5]

OR

9.a) What are the different ways in which computer buses can be used to communicate with memory and I/O? Explain.
b) What are the challenges in interrupt-driven I/O? Explain the methods for resolving the issues. [5+5]

10.a) Give an overview of methods for handling branch instructions.
b) Construct a diagram for a 4×4 omega switching network. Show the switch setting required to connect input 3 to output 1. [5+5]

OR

11.a) Demonstrate matrix multiplication on a pipeline vector processor.
b) Draw a diagram showing the structure of a 4-D hypercube network. List all the paths available from node 7 to node 9 that use the minimum number of intermediate nodes. [5+5]

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