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Code No: 821AB **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
MCA I Semester Examinations, June/July - 2018
COMPUTER ORGANIZATION

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) What is grey code? What is its importance? [5]
b) Briefly discuss memory hierarchy of a system. [5]
c) Give the instruction formats of 8086 processor. [5]
d) What are the three ways that computer buses can be used to communicate with memory and I/O? [5]
e) Illustrate the vector operations carried out on vector processors. [5]

PART - B

5 × 10 Marks = 50

2. Simplify the Boolean function F together with the don't-care conditions d in
a) sum of products form and b) product-of-sums form.
$F(w, x, y, z) = \Sigma (0,1,2,3,7,8,10)$
$d(w, x, y, z) = \Sigma (5, 6, 11, 15)$ [5+5]

OR

3. Draw the logic diagram of a 2-to-4 line decoder with only NOR gates. Include an enable input. [10]

4. Discuss organization of a 2M × 32 memory module using 512K × 8 static memory chips with a diagram. [10]

OR

5. A digital computer has a memory unit of 64K * 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words.
a) How many bits are there in the tag, index, block and word fields of the address format?
b) How many bits are there in each word of cache and how are they divided into function? Include a valid bit. [5+5]

6. What are the various addressing modes supported by 8086? Explain them with relevant instructions. [10]

OR

7. Write an assembly language program to check whether a given number is prime or not. Trace your program for two test cases. [10]

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8. Design parallel priority interrupt hardware for a system with 8 interrupt sources. [10]

OR

9. Explain the need of separate IO processor in a computer system and depict the communication between CPU and this processor. [10]

10. What is meant by pipelining? How does it improve the performance of a system? Explain with relevant examples. [10]

OR

11. Discuss cache coherence problem in multi processor system and discuss any one mechanism to address this problem. [10]

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