Code No:821AB **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
MCA I Semester Examinations, January - 2018
COMPUTER ORGANIZATION

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) Compare and contrast decoders and encoders. [5]
b) Consider a cache consisting of 256 blocks of 8 words each, for a total of 2048 words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64K words which are divided into 8192 blocks of 8 words each. Find the number of bits in Tag, Block and word field of the main memory address for direct mapping scheme.[5]
c) Give a brief note on Data transfer instructions. [5]
d) List the different methods of data transfer between the CPU and I/O devices. Explain any one in detail. [5]
e) How pipelining would improve the performance of CPU? Explain. [5]

PART - B

5 × 10 Marks = 50

2.a) Represent the Gray codes for the decimal numbers 0 to 15. What are the advantages of Gray code?
b) Explain floating point addition- subtraction unit with a neat diagram. [5+5]

OR

3.a) Draw the flowchart for Booth's algorithm for multiplication of signed 2's complement numbers and explain with an example.
b) Give a brief note on Combinational and Sequential Circuits. [5+5]

4. Suppose physical addresses are 32 bits wide. Suppose there is a cache containing 256K words of data (not including tag bits), and each cache block contains 4 words. For each of the following cache configurations,
a) direct mapped
b) 2-way set associative
c) 4-way set associative
d) fully associative
Specify how the 32-bit address would be partitioned. For example, for a direct mapped cache, you would need to specify which bits are used to select the cache entry and which bits are used to compare against the tag stored in the cache entry. [10]

OR

5.a) Discuss the different mapping techniques used in cache memories and their relative merits and demerits.
b) The access time of a cache memory is 100 ns and that of main memory is 1000 ns. It is estimated that 80% of the memory requests are for read and the remaining 20% are for write. The hit ratio for read accesses only is 0.9. A write-through procedure is used.
i) What is the average access time of the system considering only memory read cycles?
ii) What is the average access time of the system for both read and write requests? [5+5]

6. Explain the Zero, one, two, and three address instructions. [10]

OR

7. Discuss the interrupts and process control instructions in detail. [10]

8.a) What is the basic advantage of using interrupt-initiated data transfer over transfer under programmed control without an interrupt? Explain interrupt-initiated I/O in detail.

b) Why bus arbitration is required? Explain with block diagram of bus arbitration using daisy chain. [5+5]

OR

9. What is the importance of I/O interface? In a computer system, why a PCI bus is used? With a neat sketch, explain how the read operation is performed, along with the role of IRDY#/TRDY# on the PCI bus. [10]

10.a) Differentiate between a conventional scalar processor and a vector processor.

b) Describe the InterProcessor Communication and Synchronization. [5+5]

OR

11.a) What are the characteristics of multi processor.

b) What is cache coherence? [5+5]

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