R13

Code No: 811AB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
MCA I Semester Examinations, June/July - 2018
COMPUTER ORGANIZATION

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 Marks = 20

1.a) Represent the Gray codes for the decimal numbers 0 to 15. What are the advantages of Gray code? [4]
b) What is memory address map? Demonstrate with an example [4]
c) List and explain the generation of physical address. [4]
d) Why bus arbitration is required? Explain with block diagram of bus arbitration using daisy chain. [4]
e) How pipelining would improve the performance of CPU? [4]

PART - B

5 × 8 Marks = 40

2.a) Derive an algorithm in flowchart form for adding and subtracting two fixed point binary numbers when negative numbers are in signed 1's complement representation
b) Explain the BCD arithmetic operation. [4+4]

OR

3.a) Compare and contrast encoders and decoders.
b) Give a brief note on Floating point representation. [4+4]

4. A computer uses RAM chips of 1024× 1 capacity.
a) How many chips are needed, and should their address lines be connected to provide a memory capacity of 1024 bytes.
b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus. [4+4]

OR

5.a) A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.
b) Give a neat sketch that illustrates the components in a typical memory hierarchy. [4+4]

6. What is an Addressing mode? List and explain the various addressing modes with examples. [8]

OR

7.a) Write and explain the control sequence for execution of an unconditional branch instruction. 5M
b) Explain the interrupts and process control instructions. [4+4]

8. What do you mean by initialization of DMA controller? How DMA Controller works? Why does DMA have priority over the CPU when both request a memory transfer? [8]

OR

9. Compare interrupt driven data transfer scheme with DMA. Using block diagram explain interrupt driven transfer scheme [8]

10.a) What are the reasons of pipeline conflicts in pipelined processor? Discuss the various conflicts that might arise in a pipeline. How are they resolved?

b) With a neat diagram explain the pipeline for floating-point addition and subtraction.[4+4]

OR

11. Distinguish between the following
a) Pipelining and super scalar operation
b) Multiprocessors and Multi-computers. [4+4]

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