R13

Code No: 811AB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
MCA I Semester Examinations, January - 2018
COMPUTER ORGANIZATION

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 Marks = 20

1.a) What do you mean by an overflow in binary addition? How to detect the occurrence of an overflow? [4]
b) What are the major storage levels in memory hierarchy? Why do we need a memory hierarchy? [4]
c) What are assembler directives? Explain the use of 'DC' and 'DS' in 8086. [4]
d) Explain the functionalities DMA control. [4]
e) Give hypercube structure for $n = 3$. [4]

PART - B

5 × 8 Marks = 40

2.a) Construct an 8-bit adder using full adders.
b) Give the characteristic and excitation tables for SR and JK flip-flops. [4+4]

OR

3.a) Give the internal logic circuit for 4-1 multiplexer.
b) Simplify the Boolean function $AB'C + ABC' + A'BC + AB'C'$ using k-map. [4+4]

4. Explain associative memory hardware logic. [8]

OR

5.a) If the cache access time is 100ns and memory access time is 500ns and the effective access time is 10% greater than the cache access time, what is the hit ratio?
b) Give an overview of direct mapping cache assignment. [4+4]

6.a) Give an overview of INTEL 8086 program control instructions.
b) Give the sequence of actions performed on program 'CALL' and 'RETURN'. [4+4]

OR

7.a) Explain how effective address is calculated in indexed addressing and relative addressing modes using examples.
b) Write an assembly language program for computing the sum of n numbers. [4+4]

8.a) What is the need of input/output interface unit? Explain.
b) What are the different ways in which computer buses can be used to communicate with memory and I/O? [4+4]

OR

9.a) Draw a flow chart that describes the CPU-IOP communication.
b) Design parallel priority interrupt hardware for a system with eight interrupt sources. [4+4]

10.a) Instruction execution in a processor is divided into 5 stages- Instruction Fetch, Instruction Decode, Operand Fetch, Execute and Write Back. These stages take 5, 4, 20, 10 and 3 nanoseconds. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. What is the speed up achieved for 10 tasks?
b) Explain four possible hardware schemes that can be used in an instruction pipeline to minimize the performance degradation caused by instruction branching. [4+4]

OR

11. What do you mean by memory interleaving? Explain how memory interleaving can be accomplished using modular memory organization. [8]

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