Seat No.: Enrolment No._____


# GUJARAT TECHNOLOGICAL UNIVERSITY

**BE - SEMESTER– III (New) EXAMINATION – WINTER 2019**

**Subject Code: 3130704 Date: 3/12/2019**

**Subject Name: Digital Fundamentals**

**Time: 02:30 PM TO 05:00 PM Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

| | | | MARKS |
|---|---|---|---|
| **Q.1*** | **(a)** | Do as Directed<br>1. Given that $(16)_{10} = (100)_x$. Find the value of x.<br>2. Add $(6E)_{16}$ and $(C5)_{16}$.<br>3. $(1011011101101110)_2 = (\_\_\_\_\_)_8 = (\_\_\_\_\_)_{16}$. | **03** |
| | **(b)** | State and explain De Morgan's theorems with truth tables. | **04** |
| | **(c)** | Implement AND, OR, & EX-OR gates using NAND & NOR gates. | **07** |
| **Q.2** | **(a)** | Express the Boolean function F = A + B'C in a sum of minterms. | **03** |
| | **(b)** | Reduce the expression F = A [ B + C' (AB + AC')'] | **04** |
| | **(c)** | Simplify the following Boolean function by using the tabulation method.<br>F (A, B, C, D) = Σ m (0, 1, 2, 8, 10, 11, 14, 15) | **07** |
| | | **OR** | |
| | **(c)** | Using D & E as the MEV, Reduce<br>F = A'B'C' + A'B'CD + A'BCE' + A'BC'E + AB'C + ABC + ABC'D'. | **07** |
| **Q.3** | **(a)** | Simplify the Boolean function<br>F (w, x, y, z) = Σ m (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14) | **03** |
| | **(b)** | Design 1 - bit Magnitude Comparator. | **04** |
| | **(c)** | Design a full adder and realize full adder using 3X8 Decoder and 2 OR gates. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Simplify the Boolean function F = A'B'C' + B'CD' + A'BCD' + AB'C' | **03** |
| | **(b)** | Explain 4 – bit parallel adder. | **04** |
| | **(c)** | Implement the following function using 8X1 MUX<br>F (A, B, C, D) = Σ m (0, 1, 3, 4, 8, 9, 15) | **07** |
| **Q.4** | **(a)** | Explain SR flip-flop using characteristic table & characteristic equation. | **03** |
| | **(b)** | Explain the working of SISO shift register. | **04** |
| | **(c)** | Design a counter with the following binary sequence: 0, 1, 3, 7, 6, 4 and repeat. Use T – flip-flops. | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | What is the race around condition in JK flip-flop? | **03** |
| | **(b)** | Design 4-bit Ring counter using D flip-flip. | **04** |
| | **(c)** | Design JK flip-flip using D flip-flip. | **07** |
| **Q.5** | **(a)** | Explain the specification of D/A converter. | **03** |
| | **(b)** | Explain R-2R ladder type D/A converter, | **04** |
| | **(c)** | Explain Successive Approximation type A/D converter. | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | Explain classification of Memories. | **03** |
| | **(b)** | Explain the types of ROM. | **04** |
| | **(c)** | A combinational circuit is defined by the function<br>$F_1$ (A, B, C,) = Σ m (4, 5, 7) $F_2$ (A, B, C,) = Σ m (3, 5, 7)<br>Implement the circuit with a PLA having 3 inputs, 3 product term & 2 outputs. | **07** |

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