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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (New) EXAMINATION – WINTER 2019

Subject Code: 3130907 Date: 30/11/2019

Subject Name: Analog & Digital Electronics

Time: 02:30 PM TO 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			Marks
Q.1	**(a)**	What is ideal differential amplifier?	**03**
	(b)	Design half adder circuit.	**04**
	(c)	Compare different types of power amplifiers.	**07**
Q.2	**(a)**	Calculate maximum frequency for a sine wave, output voltage of 12 V peak with an OPAMP having slew rate 1 V/µS.	**03**
	(b)	Prove that voltage follower has unity gain.	**04**
	(c)	Draw integrator circuit with example of input and output waveforms. Derive expression for output voltage.	**07**
		OR	
	(c)	Write short note on Wien bridge oscillator using OPAMP.	**07**
Q.3	**(a)**	Explain zero crossing detector.	**03**
	(b)	Explain how to generate triangular wave using OPAMP.	**04**
	(c)	Explain first order Butterworth low-pass filter. Derive expression of filter gain.	**07**
		OR	
Q.3	**(a)**	Explain window comparator.	**03**
	(b)	Draw Schmitt trigger circuit. Plot input and output waveforms.	**04**
	(c)	Explain positive peak detector circuit using OPAMP.	**07**
Q.4	**(a)**	What is multiplexer?	**03**
	(b)	Classify digital logic gates. Draw truth table and symbols of basic logic gates.	**04**
	(c)	Design a combinational circuit which has 3 bit binary input and has output as square of inputs.	**07**
		OR	
Q.4	**(a)**	Design full adder circuit.	**03**
	(b)	Describe POS and SOP with example.	**04**
	(c)	Explain in detail 7 segment LED display.	**07**
Q.5	**(a)**	Explain digital to analog converter with binary weighted resisters.	**03**
	(b)	Explain positive edge triggered JK flip-flop.	**04**
	(c)	Explain 4 bit ring counter using waveforms.	**07**
		OR	
Q.5	**(a)**	What are preset and clear inputs with flip-flops? Why are they provided?	**03**
	(b)	Explain master slave JK flop-flop.	**04**
	(c)	Design a 4 bit synchronous up counter.	**07**

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