Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (New) EXAMINATION – WINTER 2019

Subject Code: 3131102 **Date: 30/11/2019**

Subject Name: Digital System Design

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	State and prove De Morgan's theorem for 2 variables.	**03**
	(b)	Differentiate between combinational and sequential circuits.	**04**
	(c)	Design 4-bit binary to Grey code converter circuit and draw the logic diagram.	**07**
Q.2	**(a)**	Define canonical and standard forms of Boolean function and give their examples.	**03**
	(b)	Convert 375.125 into base 2, base 8, base 16 and BCD.	**04**
	(c)	Simplify the Boolean function F(A,B,C,D)= ∑(1,3,7,11,15) using K-map if don't care conditions are 0, 2 and 5. Draw the simplified logic diagram only using NAND gates.	**07**
		OR	
	(c)	Compare TTL, ECL and CMOS logic families and draw CMOS inverter logic circuit.	**07**
Q.3	**(a)**	Define: Encoder, Decoder, De-multiplexer.	**03**
	(b)	Describe full adder circuit with truth table and logic diagram.	**04**
	(c)	Implement the Boolean function F(W,X,Y,Z)= ∑(0,1,3,4,8,9,15) using suitable multiplexer.	**07**
		OR	
Q.3	**(a)**	Briefly explain the steps for VLSI design flow.	**03**
	(b)	Define a parity bit and design 3-bit odd parity generator circuit.	**04**
	(c)	Describe working principle of Programmable Logic Array with block diagrams.	**07**
Q.4	**(a)**	Derive excitation tables for R-S, J-K and T flip-flops.	**03**
	(b)	Discuss working of clocked delay type flip-flop with characteristic table and logic diagram.	**04**
	(c)	Describe the operation of 4-bit bidirectional shift register with logic diagram.	**07**
		OR	
Q.4	**(a)**	Define: Register, Ripple counter, Synchronous counter.	**03**
	(b)	Explain working of Toggle flip-flop with characteristic table and logic diagram.	**04**
	(c)	Design a counter that counts the sequence as 0, 1, 2, 4, 5, 6 and rolls over to 0 again. Use +ve edge triggered J-K flip-flops.	**07**
Q.5	**(a)**	Compare asynchronous and synchronous state machines.	**03**
	(b)	Discuss general state machine architecture.	**04**
	(c)	Define state table & state diagram. Draw state diagram of a state	**07**

machine with state table as given in Table-1. The state machine contains input variable X and output variable Y and two flip-flops A & B.

OR

Q.5 **(a)** Discuss working fundamentals behind FINFET. **03**

(b) State various types of D/A converters and briefly explain any one of them. **04**

(c) Explain dual slope type A/D converter in detail. **07**

Present State AB	**Next State AB**		**Output Y**	
	X=0	**X=1**	**X=0**	**X=1**
00	00	01	0	0
01	11	01	0	0
10	10	00	0	1
11	10	11	0	0

Table-1.

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