Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (Old) EXAMINATION – WINTER 2019

Subject Code: 131101 **Date: 30/11/2019**

Subject Name: Basic Electronics

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** **Answer the following questions:** **07**

1) Sketch the piecewise linear characteristics of PN junction diode.

2) What is cut-in voltage? Write approx. value of cut-in voltage for silicon and germanium diode.

3) Define Thermal resistance.

4) Define Mean life time of a carrier.

5) What do you mean by PIV (Peak Inverse voltage)? Enlist the value of PIV for different rectifiers.

6) What is depletion region in PN junction diode.

7) Explain Zener breakdown phenomena.

(b) Explain the Hall effect and obtain the expression of Hall coefficient. List the applications of Hall effect. **07**

Q.2 **(a)** Draw and explain bridge rectifier circuit with capacitor filter. Draw necessary waveforms. **07**

(b) The resistivity of intrinsic silicon is 3×10^5 Ω-cm at 30°C. Calculate the intrinsic concentration at 100°C. Assume $\mu_n=0.13m^2$/V-sec and $\mu_p=0.05m^2$/V-sec at 30°C. **07**

OR

(b) A silicon sample is non-uniformly doped with donor impurity of $10^{14}m^{-3}$. A current density of $10mA/cm^2$ is generated when electric field of 3V/cm is applied across it. Find the concentration gradient at 27°C. Given: $\mu_n=1500\ cm^2$ /V-sec. **07**

Q.3 **(a)** Draw the circuit of Common Emitter configuration of transistor. Explain input and output characteristics. Also derive $\alpha = \beta / \beta+1$. **07**

(b) For the circuit shown in **Figure (1)**,explain working of the circuit and draw output waveform for given input signal. Also draw transfer characteristics. **07**

OR

Q.3 **(a)** What is biasing? Why biasing is required for transistor? List biasing methods for transistor. Draw and explain the circuit of voltage divider biasing **07**

(b) The silicon transistor used in the circuit of **Figure (2)** has $VCE_{(sat)}=0.2V$, $VBE_{(sat)}=0.8V$, $VBE_{(active)}= 0.7V$, $VBE_{(cut\ in)}=0.5V$ and $\beta=100$. **(I)** Show that the transistor is in saturation. **(II)** Calculate the value of RE for which the transistor just comes out of saturation. **07**

Q.4 **(a)** Define stabilization factors; S, S', and S". Also derive expressions for S and S' for self bias transistor circuit. **07**

(b) The transistor used in the circuit of **Figure (3)** has the following parameters: hie = 500 Ω, hre = 2.4×10^{-4}, hfe = 60 and hoe = 1/40 k. Calculate : [1]Vo/VS [2] R'_i [3] R'_o. Assume all capacitors to be very large. **07**

OR

Q.4 **(a)** Draw circuit of an idealized class B push pull power amplifier and explain its operation with the help of necessary waveforms. **07**

(b) Calculate the dc bias voltages and currents for the circuit shown in **Figure (4).** **07**

Q.5 **(a)** Derive expressions for A_I, R_i, A_V and Y_o in terms of CE h-parameters for emitter follower circuit. **07**

(b) Draw and explain working of diode compensation circuit for V_{BE} for self-stabilization in amplifier circuit. **07**

OR

Q.5 **(a)** Draw structure of n-channel JFET and explain its working. **07**

(b) Draw a structure of p-channel MOSFET. Explain its working for enhancement type. Also draw and explain drain characteristics and transfer curve for the same device. **07**

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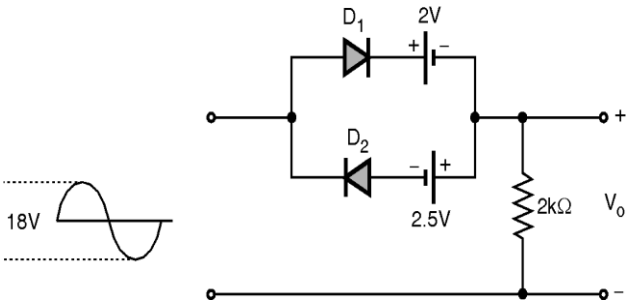

Figure (1)

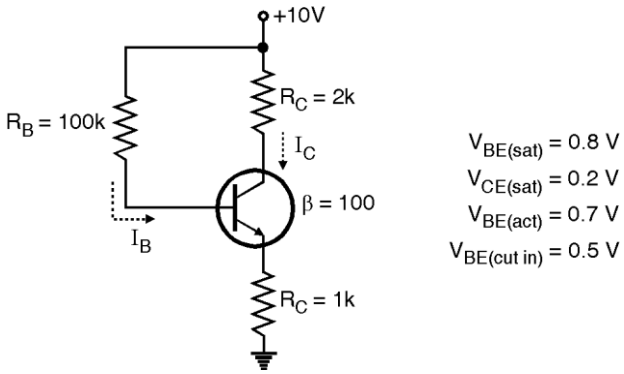

Figure (2)

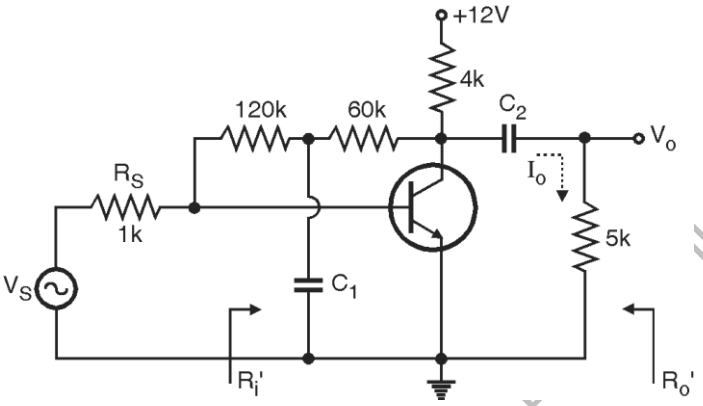

Figure (3)

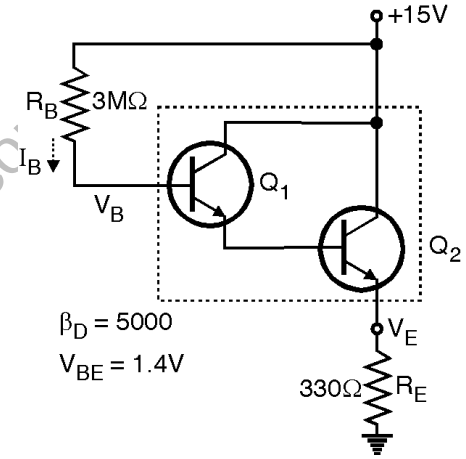

Figure (4)