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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– IV (New) EXAMINATION – WINTER 2019

Subject Code: 2140910 **Date: 10/12/2019**

Subject Name: Digital Electronics

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1		Do as instructed (Each question carry two marks)	**14**
	(a)	How to convert Binary to Gray Code? Explain with necessary diagrams.	
	(b)	Convert: $(ABC)_{16}$ = ( )$_{10}$ = ( )$_{8}$	
	(c)	Add $(-258)_{10}$ to $(-48)_{10}$ using 2's compliments method.	
	(d)	Subtract $(108)_{10}$ from $(93)_{10}$ using 2's compliments method.	
	(e)	Add $(-7)_{10}$ to $(-8)_{10}$ using 1's compliments method.	
	(f)	Convert $(4500)_{10}$ = ( )$_{16}$ = ( )$_{8}$	
	(g)	Define Excess - 3 code with suitable example.	
Q.2	**(a)**	Explain TTL logic family with necessary sketches and truth table.	**03**
	(b)	Define universal gates. Design different types of gate using each universal gates.	**04**
	(c)	Design & explain full subtractor with truth table and circuit diagrams.	**07**
		OR	
	(c)	Design & explain two half adder can make one full adder with truth table and circuit diagrams.	**07**
Q.3	**(a)**	Explain following with examples 1. Minterm 2. Maxterm 3. Don't care	**03**
	(b)	Reduce the following function using K-map. Y = ∑m (0,2,4,6,9,13,21,23,25,29,31)	**04**
	(c)	Reduce the following function using tabulation method Y = ∑m (0,2,3,6,7,8,9,10,13)	**07**
		OR	
Q.3	**(a)**	Explain following with examples 1. POS 2. SOP	**03**
	(b)	Demonstrate the validity of the De Morgan's theorems by truth tables.	**04**
	(c)	Reduce following function with help of Boolean expression. Also realize the expression with NAND gate. Y = (A+B) (A+(B'+C')') +A' (B+C)	**07**
Q.4	**(a)**	Derive Excitation tables for J-K flip flop.	**03**
	(b)	Explain SIPO shift register with necessary circuit diagram.	**04**
	(c)	Explain J - K master slave flip flop with necessary sketches and truth table.	**07**
		OR	
Q.4	**(a)**	Derive Excitation tables for S-R flip flop.	**03**
	(b)	Explain PIPO shift register with necessary circuit diagram.	**04**
	(c)	Design modulo - 10 counter with timing diagrams.	**07**
Q.5	**(a)**	Define following terms: 1. Resolution 2. Linearity 3. Accuracy	**03**

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	(b)	Explain PROM & Flash memory.	**04**
	(c)	Explain R -2R ladder method for D/A converter with necessary circuit diagrams.	**07**

OR

Q.5	**(a)**	Explain Sample and Hold circuit.	**03**
	(b)	Write a short note on memory organization.	**04**
	(c)	Explain successive approximation method for A/D converter with circuit diagram.	**07**

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