Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– VI (New) EXAMINATION – WINTER 2019

Subject Code: 2160909 **Date: 12/12/2019**

Subject Name: Advance Microcontrollers

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	List advantage and disadvantages of Harvard Architecture over Von Neumann architecture	**03**
	(b)	Give the significance of C compiler, Debugger, Assembler and Flash programmer	**04**
	(c)	Why Watch-dog timer is necessary for embedded systems? Explain the watchdog timer of P89V51RD2 in detail	**07**
Q.2	**(a)**	Draw PCA interrupt system of P89V51RD2	**03**
	(b)	List out steps required to enable interrupts safely in an IRQ handler	**04**
	(c)	Draw and explain block diagram of MPC 3304(ADC).	**07**
		OR	
	(c)	Explain what is PWM? Write an embedded C program to generate PWM in xx51 microcontroller. Assume necessary data and clearly mention your assumptions.	**07**
Q.3	**(a)**	Differentiate ISP (In System Programming) and IAP (In Application Programming).	**03**
	(b)	Explain the CMOD, CCON registers of P89V51RD2.	**04**
	(c)	Discuss I2C & SPI communication protocol for microcontrollers.	**07**
		OR	
Q.3	**(a)**	Explain the SPI control & SPI status registers in P89V51RD2	**03**
	(b)	Explain PWM mode of P89V51RD2 PCA timer in detail.	**04**
	(c)	Discuss the pulse width modulator mode of 89V51RD2 microcontroller with C programming code	**07**
Q.4	**(a)**	Explain Round Robin with Interrupt Architecture.	**03**
	(b)	Explain multi-AHB bus matrix in STM32F4XX.	**04**
	(c)	Explain the NVIC operation exception entry and exit of STM32F4XX	**07**
		OR	
Q.4	**(a)**	Explain pointer to structure with example	**03**
	(b)	Draw and explain reset circuit of STM32F4xx.	**04**
	(c)	Explain the feature of GPIO in detail.	**07**
Q.5	**(a)**	Explain the concept of memory segmentation in Cortex processor.	**03**
	(b)	Explain the main feature of TIM6 & TIM7 in STM32F4XX	**04**
	(c)	Explain the bit banding technique in cortex M processors	**07**
		OR	
Q.5	**(a)**	What is Enumerator?	**03**
	(b)	Explain tail chaining in cortex M processors.	**04**
	(c)	Explain the 3-stage pipelining in cortex CPU	**07**

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