Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– III (New) EXAMINATION – WINTER 2019

Subject Code: 2130306 **Date: 5/12/2019**

Subject Name: Fundamentals of Digital Design

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Convert number $(10.11)_2$ into decimal, hexa and octal numbers.	**03**
	(b)	Draw the symbol and truth tables of Ex-OR, Ex-NOR, NAND and NOR logic gates.	**04**
	(c)	Simplify the function F=∑(0,3,4,6,8,10,12,14) with and without don't care conditions d=∑(1,2,9,11) and compare results.	**07**
Q.2	**(a)**	Give the full form of DL, RTL, DTL, TTL, ECL logic family.	**03**
	(b)	Define terms: fan-in, fan-out, switching times and noise margin.	**04**
	(c)	Simplify the following Boolean functions to a minimum numbers of literals. 1. F1 = XYZ+X'Y+XYZ' 2. F2 = (X+Y+Z)(X)(Y)(Z) 3. F3 = X+XY+XYZ+XY'+XZ' 4. F4 = A´B´C´+B´CD´+A´BCD´+AB´C´	**07**
		OR	
	(c)	Simplify the Boolean Function by using the tabulation method: F = Σ(0,1,2,8,10,11,14,15)	**07**
Q.3	**(a)**	Explain De Morgan's Theorem and prove it.	**03**
	(b)	Perform (-8) –(-4) using 2's complement method.	**04**
	(c)	Implement the function F= D(A+BC)+AB' using NOR gates.	**07**
		OR	
Q.3	**(a)**	Design and explain half adder circuit.	**03**
	(b)	Explain operation of 4:1 multiplexer with logic diagram & truth table.	**04**
	(c)	Design a BCD adder using 4 bit parallel adder blocks and basic gates.	**07**
Q.4	**(a)**	Explain types of ROMs.	**03**
	(b)	Explain working of JK- flip-flop with diagram.	**04**
	(c)	Design 4-bit binary to BCD code convertor.	**07**
		OR	
Q.4	**(a)**	Define PLA with block diagram.	**03**
	(b)	Write a short note on shift register.	**04**
	(c)	Design and explain 4 bit magnitude comparator.	**07**
Q.5	**(a)**	Draw and explain RS flip flop.	**03**
	(b)	Explain R-2R ladder type DAC.	**04**
	(c)	Draw and explain 3 bit binary counter using JK flip flop.	**07**
		OR	
Q.5	**(a)**	Explain state diagram with example.	**03**
	(b)	Explain successive approximation type ADC.	**04**
	(c)	What is the full form of FPGA? Explain the basic block diagram of FPGA.	**07**

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