Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– VI (New) EXAMINATION – WINTER 2019

Subject Code: 2161101 **Date: 11/12/2019**

Subject Name: VLSI Technology & Design

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

			MARKS
Q.1	**(a)**	Draw VLSI design flow with block diagram.	**03**
	(b)	Differentiate between FPGA and CPLD	**04**
	(c)	Discuss various packaging technology used for VLSI chips.	**07**
Q.2	**(a)**	Explain the concept of MOSFET as a switch.	**03**
	(b)	Justify that size of PMOS transistor chosen to be 2.5 times of an NMOS transistor.	**04**
	(c)	Design a resistive load inverter with RL=1KΩ, such that VOL = 0.6V. The enhancement type driver transistor has the following parameters: V_{dd} = 5V, V_{To} = 1V, γ = 0.2 V1/2, λ =0, $\mu_n C_{ox}$ = 22 μA/V^2. Determine i) Require aspect ratio. W/L ii) V_{IL} and V_{IH} and iii) noise margin NM_L and NM_H	**07**
		OR	
	(c)	Draw the inverter circuit with depletion type nMOS load. Mention the operating regions of driver and load transistors for different input voltages. Derive the expression of critical voltages V_{IL},V_{OL},V_{IH},V_{OH}.	**07**
Q.3	**(a)**	Define following Terms: (i) Threshold Voltage (ii) Noise Margin (iii) Propagation Delay	**03**
	(b)	Explain: Substrate bias effect.	**04**
	(c)	Explain the energy band diagram of MOS structure at surface inversion and derive the expression for the maximum possible depth of the depletion region.	**07**
		OR	
Q.3	**(a)**	Draw CMOS Inverter circuit and voltage transfer characteristics. Mention different operating region of NMOS and PMOS on VTC.	**03**
	(b)	Derive expression for frequency of oscillation for three stage ring oscillator circuit. Draw necessary circuit and waveforms.	**04**
	(c)	Derive the expression of τ_{PHL} of a CMOS inverter using differential equation method.	**07**
Q.4	**(a)**	Discuss the effect of Full scaling(constant-Field scaling) on: (i) Cox (ii) I_D	**03**
	(b)	Derive Req of all regions in CMOS Transmission gates	**04**
	(c)	Implement and Describe CMOS clocked RS flip-flop.	**07**

OR

Q.4	**(a)**	Draw two-input CMOS NOR and NAND gate circuits.	**03**
	(b)	Which are the four general criteria to measure design quality of a fabricated integrated circuit (chip)? Briefly explain each of them.	**04**
	(c)	Realize the following Boolean function using CMOS Transmission Gates. F = AB + A'C' + AB'C	**07**
Q.5	**(a)**	Draw the circuit diagram of domino CMOS logic gate.	**03**
	(b)	Explain Voltage bootstrapping.	**04**
	(c)	Implement and Describe CMOS clocked JK flip-flop.	**07**

OR

Q.5	**(a)**	Draw general layout of an H-tree clock distribution network.	**03**
	(b)	Describe in brief : Built in Self Test (BIST)	**04**
	(c)	What is Latch up? Explain the prevention techniques.	**07**

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