Seat No.: _____  Enrolment No. 

# GUJARAT TECHNOLOGICAL UNIVERSITY

**BE - SEMESTER– III (New) EXAMINATION – WINTER 2019**

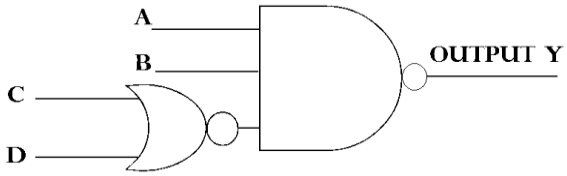
**Subject Code: 2131004** **Date: 3/12/2019**

**Subject Name: Digital Electronics**

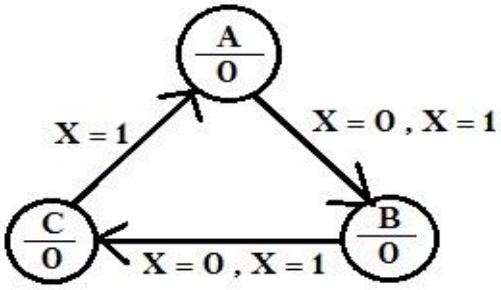
**Time: 02:30 PM TO 05:00 PM** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

| | | | MARKS |
|---|---|---|---|
| **Q.1** | **(a)** | **Answer the following Questions:**<br>**1.** Find 2's Complement Representation of $(-52)_{10}$ .<br>**2.** Convert the binary number $(1101110.0110)_2$ to decimal.<br>**3.** For a given logic circuit, if A=B=1, and C=D=0. Find output Y.<br>  | **03** |
| | **(b)** | Minimize the following Boolean expression using Karnaugh Map (K-MAP) and Draw the draw the simplified logic circuit diagram.<br>$Y= \sum m(0,1,5,9,13,14,15) + d(3,4,7,10,11)$ | **04** |
| | **(c)** | Explain full subtractor and construct full subtractor using half subtractors. | **07** |
| **Q.2** | **(a)** | **Define Following Terms.**<br>1. Nibble 2. Negative Logic 3. Even Parity | **03** |
| | **(b)** | Implement 16 X 1 multiplexer using 2 X 1 multiplexer. | **04** |
| | **(c)** | With a neat block diagram explain the function of encoder. Explain priority encoder? | **07** |
| | | **OR** | |
| | **(c)** | Design a combinational logic circuit such that output is high, when four bit binary number is greater than $(0110)_2$. | **07** |
| **Q.3** | **(a)** | Design 3-bit Binary to Gray code Converter. | **03** |
| | **(b)** | Explain 3-bit synchronous Binary Up counter with timing diagram. | **04** |
| | **(c)** | Explain T Flipflop with Excitation Table. Implement T flip flop using SR flip flop. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Distinguish between combinational and Sequential logic circuits. | **03** |
| | **(b)** | Draw and Explain 4-bit bidirectional Shift Register. | **04** |
| | **(c)** | Differentiate the Asynchronous counter and Synchronous counter. Explain 3- bit up/down Asynchronous counter in detail. | **07** |
| **Q.4** | **(a)** | State the advantages of Finite State Machine. | **03** |
| | **(b)** | Which are the various problems of Asynchronous Circuits? | **04** |

**(c)** Realize the sequential circuit for the state diagram shown in figure. **07**




**OR**

**Q.4** **(a)** Define State Table and State Diagram. **03**

**(b)** Describe General State Machine Architecture with suitable diagrams. **04**

**(c)** Explain the Fundamental Mode Model of ASM with Suitable example. **07**

**Q.5** **(a)** Compare the Following in every aspect: TTL and CMOS **03**

**(b)** Explain oscillation problem of an asynchronous state machines with the help of one example. **04**

**(c)** Write short note on Programmable Logic Arrays. . **07**

**OR**

**Q.5** **(a)** Define following terms with respect to Finite State Machine. **03**

1. Melay machine 2. Moore machine.

**(b)** Draw and explain the working operation of 2- INPUT TTL NAND gate. **04**

**(c)** Compare ROM, PLA and PAL. **07**

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