Seat No.: _____ Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– VII (New) EXAMINATION – WINTER 2019

Subject Code: 2172409 **Date: 03/12/2019**

Subject Name: Digital Signal Processing for Power Electronics

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Differentiate Energy signal and Power signal.	**03**
	(b)	Enlist applications of DSP.	**04**
	(c)	Classify and explain types of systems with examples.	**07**
Q.2	**(a)**	Check the system described by equation y(t) = sinx(t) for time variant.	**03**
	(b)	Enlist standard Discrete time signal with neat sketches.	**04**
	(c)	What is MAC? Explain it and state its importance with reference to DSP.	**07**
		OR	
	(c)	Draw and explain the block diagram of architecture for modified Harvard digital signal processor.	**07**
Q.3	**(a)**	State relation between Fourier Transform & Z-Transform.	**03**
	(b)	Find the N point DFT for $x(n) = a^n$ for $0<a<1$	**04**
	(c)	What do you understand by twiddle factor? Derive the relationship between DFT and Z Transform.	**07**
		OR	
Q.3	**(a)**	Explain any three property of DFT.	**03**
	(b)	Determine the periodicity of the following signal. (1) $x_1(t) = \sin 15\pi t$ (2) $x_2(t) = \sin 20\pi t$ (3) $x_3(t) = x_1(t) + x_2(t)$	**04**
	(c)	Find x(n) if $X(z) = \frac{1+0.5z^{-1}}{1-0.5z^{-1}}$	**07**
Q.4	**(a)**	Define sampling and aliasing.	**03**
	(b)	Draw the structure of cascade realization of $H(z) = \frac{(1-z^{-1})^3}{(1-0.5z^{-1})(1-0.125z^{-1})}$	**04**
	(c)	Explain following. (1) Radix-2 FFT algorithm (2) DIT algorithm.	**07**
		OR	
Q.4	**(a)**	Discuss the need of interlocking in brief.	**03**
	(b)	Draw the structure of parallel realization of $H(z) = \frac{(1-z^{-1})^3}{(1-0.5z^{-1})(1-0.125z^{-1})}$	**04**
	(c)	Find the inverse DFT of X(k) = {1,2,3,4}.	**07**
Q.5	**(a)**	Explain the concept of pipelining in DSP.	**03**
	(b)	How reduction in product round off errors is achieved?	**04**

	(c)	With neat diagram, explain the structures for realization of FIR systems.	**07**

OR

Q.5	**(a)**	Explain in brief the fixed point representation of binary numbers.	**03**
	(b)	What are the different formats of fixed point representation?	**04**
	(c)	Explain the structures for realization of IIR systems.	**07**

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