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GUJARAT TECHNOLOGICAL UNIVERSITY

		BE - SEMESTER- III (New) EXAMINATION - WINTER 2019	
Subi	ect (Code: 2131704 Date: 3/12/2019)
Subject Name: Digital Logic Circuits			
Subj T	Fimo, 02.20 DM TO 05.00 DM		
1 Ime: 02:50 PM 10 05:00 PM 10 tal Marks:			U
Instructions:			
	1.	Attempt all questions.	
	2. 2	Make suitable assumptions wherever necessary.	
	з.	Figures to the right indicate run marks.	
01	(a)	What is Race condition?	03
Q.1	(a) (h)	Define : 1) Ean in 2) Ean out	03
	(0)	3) Propagation Delay 4) Noise margin	04
	(-)	State and Drass Da Managar's the same	07
	(C)	State and Prove De Morgan's theorem.	07
0.2	(8)	Write a short note on PLA.	03
×	(\mathbf{b})	Convert the following	04
	(~)	i. Decimal number 256 to Hexadecimal equivalent.	• -
		ii. Decimal number 648 to octal equivalent.	
	(c)	Draw logic diagram, symbol and characteristic table for JK flip-flop.	07
	(0)	OR	0.
	(c)	Explain positive edge-triggered D flip-flop.	07
Q.3	(a)	Explain state table, state diagram with example.	03
-	(b)	Design full subtractor using half subtractors.	04
	(c)	With the help of a neat diagram, explain the working of a two-input TTL	07
		NAND gate.	
		OR	
Q.3	(a)	Realize Ex-OR gate and NOT gate using NOR gate.	03
	(b)	Reduce the expression:	04
		I. A[B + $\overline{C}(\overline{AB + A\overline{C}})$]	
		$II \left(\overline{A + \overline{BC}} \right) \left(A\overline{B} + ABC \right)$	
	(c)	Explain BCD-to-Seven segment decoder	07
04	(\mathbf{c})	Draw neat diagram of 3x8 decoder circuit	03
2.1	(\mathbf{u})	Simplify the Boolean function using K-map.	04
	(0)	$F(w \ge vz) = \sum m(0.1.2.4.5.6.8.9.12.13.14)$	•••
	(c)	Explain with logic diagram of 4-bit serial-in serial-out shift register	07
	(•)	OR	•••
0.4	(8)	Write a short note on shift register.	03
x	(b)	Write a short note on Arithmetic micro operation in detail.	04
	(c)	Explain 4-bit ring counter with circuit diagram and waveforms.	07
0.5	(a)	Convert SR flip-flop into T flip-flop.	03
	(b)	Draw neat diagram of 2-bit magnitude comparator circuit.	04
	(c)	Write the state table and state equation with the state diagram of clocked D	07
	(2)	flip-flop.	
		OR	
0.5	(a)	Explain 2 bit binary UP counter using JK flip-flops.	03
C	(h)	Distinguish between combinational and sequential switching circuits.	04
	(c)	Explain Successive Approximation ADC.	07
	(-)	1 rr	
