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GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– VIII (New) EXAMINATION – WINTER 2019

Subject Code: 2181107 **Date: 21/11/2019**

Subject Name: Testing And Verification

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Discuss yield in detail.	**03**
	(b)	Enlist the objectives for creating Test Bench.	**04**
	(c)	Differentiate following terms: Testing and Verification	**07**
Q.2	**(a)**	Discuss significance of Design for Testability.	**03**
	(b)	Discuss following terms: Controllability and Observability	**04**
	(c)	Explain transistor faults in detail with the help of example.	**07**
		OR	
	(c)	Explain stuck-at-faults in detail with the help of example.	**07**
Q.3	**(a)**	Draw level-sensitive muxed-D scan cell design.	**03**
	(b)	Enlist various algorithms for fault simulation	**04**
	(c)	Discuss typical scan design flow with the help of flowchart.	**07**
		OR	
Q.3	**(a)**	Enlist various popular scan architectures with functionality.	**03**
	(b)	Explain RTL testability repair design flow.	**04**
	(c)	Discuss various scan design rules.	**07**
Q.4	**(a)**	Differentiate fault simulation and logic simulation.	**03**
	(b)	Discuss Hazard. Enlist different types of Hazards.	**04**
	(c)	Explain Logic simulation for design verification in detail.	**07**
		OR	
Q.4	**(a)**	Compare: Event-Driven Simulation and Compiled-Code Simulation	**03**
	(b)	How would you detect hazard? Explain in detail with one example circuit.	**04**
	(c)	Explain probability-based Testability analysis with 3 input AND gate.	**07**
Q.5	**(a)**	Discuss role of verification plan.	**03**
	(b)	Discuss various levels of verification.	**04**
	(c)	List down different verification methods and explain any one in detail.	**07**
		OR	
Q.5	**(a)**	Discuss various challenges for Functional verification of VLSI circuits.	**03**
	(b)	SystemVerilog is preferred over other Hardware Verification Languages to implement Test benches in industry. Why?	**04**
	(c)	Write Types of Test Benches. Explain any one with example	**07**

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