Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI(NEW) – EXAMINATION – SUMMER 2019

Subject Code:2160909 Date:21/05/2019

Subject Name:Advance Microcontrollers

Time:10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain CMOD and CCON registers in PCA timer.	**03**
	(b)	Enlist features of P89V51RD2.	**04**
	(c)	Explain the feature of GPIO in STM32F4xx.	**07**
Q.2	**(a)**	Discuss I-bus, D-bus and S-bus in STM32F4XX.	**03**
	(b)	Explain the SPI control & SPI status registers in P89V51RD2.	**04**
	(c)	Explain the round robin with interrupt architecture.	**07**
		OR	
	(c)	Discuss the concept of PCA timer and explain capture mode of PCA timer.	**07**
Q.3	**(a)**	Explain the main feature of TIM6 & TIM7 in STM32F4XX.	**03**
	(b)	What is interrupt pre-emption in cortex-M Processor family?	**04**
	(c)	Explain the NVIC operation exception entry and exit of STM32F4XX.	**07**
		OR	
Q.3	**(a)**	Explain GPIO port mode register (GPIOx_MODER).	**03**
	(b)	Explain tail chaining in cortex M processors.	**04**
	(c)	Explain Thumb 2 Instruction set of ARM CORTEX.	**07**
Q.4	**(a)**	Compare Von Neumann and Harvard architecture.	**03**
	(b)	Explain the bit banding technique in cortex M processors.	**04**
	(c)	Explain the 3-stage pipelining in cortex CPU.	**07**
		OR	
Q.4	**(a)**	What do you mean by enumerator?	**03**
	(b)	Draw & explain the input configuration of GPIO in STM32F4XX.	**04**
	(c)	Explain high speed output toggle mode of PCA timer.	**07**
Q.5	**(a)**	Describe the importance of watchdog timer in embedded system.	**03**
	(b)	Draw master-slave SPI protocol and explain associated signals.	**04**
	(c)	Draw and explain Multi-AHB bus matrix.	**07**
		OR	
Q.5	**(a)**	Explain the systick timer in ARM CORTEX.	**03**
	(b)	Draw PCA interrupt system of P89V51RD2.	**04**
	(c)	Discuss about the concept of I2C communication protocol.	**07**

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